LOONGSON

2P0500

V1.02

0 0

2P0500

1

2P0500 / SOC

A4

2P0500

2P0500

LA364 64 L1 Cache(I/D) 32KB L2 Cache 512KB 750MHz

LA132 32 400MHz

1 32 DDR3

2 10M/100M/1000M GMAC RGMII/MII

3 USB2.0 HOST 1 OTG

4 SPI 1

1 8 LSU

1 1 AFE/CIS

1 4 8 DA

4 I2C

8 UART

2 SDIO

40 PWM

3 PMIO

139 GPIO

1

RTC/HPET

DFS/DPM

1.1

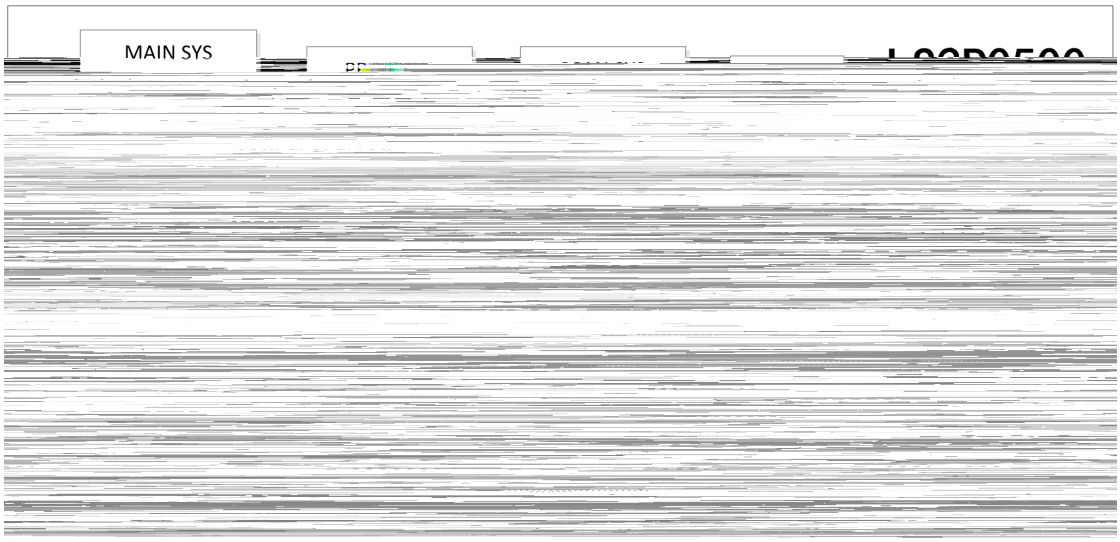
2P0500

Cache IO Cache Cache IODMA

GMAC USB IMAGE PRINT SCAN

I2C UART

2P0500 1-1



1.1 2P0500

1.2

1.2.1

LA364 LA132

LoongArch

1 64

32KB Cache 32KB Cache

512KB Cache

I/O DMA Cache

JTAG

1.2.2

32 DDR3 400MHz

32/16

1.2.3 USB

3 USB2.0 HOST

1 OTG

USB1.1 USB2.0

EHCI 480Mbps

OHCI

1.2.4 GMAC

10/100/1000Mbps MAC

IEEE 802.3

PHY RGMII/MII

/

Timestamp

CSMA/CD

CRC

1.2.5 SPI

4

(SPI0)

I/O SPI Flash

1.2.6 **UART**

1 UART TXD,RXD,CTS, RTS, DSR,DTR,DCD, RI

8 UART

1.2.11 PMIO

3 PMIO

80 1 1 o ѽ ž

1.2.18

( ) -10℃ 70℃( )

1.2.19

1.3

1-1

		( )	

1.4

1.4.1

N/n

N/n RTC RTC

SOC

1.4.2

1-2

A	
DIFF I/O	
DIFF IN	
DIFF OUT	
I	
I/O	
O	
OD	
P	
G	

1.4.3

16 ’hxxx 2 ’bxx 10

DDR_DQ0, DDR_DQ1, …

DDR_DQ[31:0]

1.4.4

[ ].[ ] chip_config0.uart_split

0 chip_config0 uart_split

2

2.1 DDR3

DDR_DQ[31:0]	I/O	’hx		VDDIO_DDR		
DDR_DQSP[3:0] DDR_DQSN[3:0]	DIFF I/O	’hx		VDDIO_DDR		
DDR_DQM[3:0]	O	’hx		VDDIO_DDR		
DDR_A[15:0]	O	’hx		VDDIO_DDR		
DDR_BA[2:0]	O	’hx		VDDIO_DDR		
DDR_WEN	O	’hx		VDDIO_DDR		
DDR_CASN	O	’hx		VDDIO_DDR		
DDR_RASN	O	’hx		VDDIO_DDR		
DDR_SCSN0	O	’hx		VDDIO_DDR		
DDR_CKE0	O	’hx		VDDIO_DDR		
DDR_CKP0 DDR_CKN0	DIFF OUT	’hx		VDDIO_DDR		
DDR_ODT0	O	’hx		VDDIO_DDR		
DDR_RESETN	O	’hx		VDDIO_DDR		

2.2 GMAC

GMAC[1:0]_TX_CLK_O	O	’h0		VDD_3V3		
GMAC[1:0]_TX_CLK_I	I			VDD_3V3		
GMAC0_TX_CTL	O	’h0		VDD_3V3		
GMAC0_TXD[3:0]	O	’h0		VDD_3V3		
GMAC[1:0]_RX_CLK_I	I			VDD_3V3		
GMAC0_RX_CTL	I			VDD_3V3		
GMAC0_RXD[3:0]	I			VDD_3V3		
GMAC0_MDCK	O	’h0		VDD_3V3		
GMAC0_MDIO	I/O	’hx		VDD_3V3		

2P0500 RGMII MII

GMAC_TX_CTL	GMAC_TX_CTL	GMAC_TX_EN
GMAC_RX_CTL	GMAC_RX_CTL	GMAC_RX_DV
GMAC_TX_CLK_O	GMAC_TX_CLK_O( )	GMAC_RX_ER( )
-	-	GMAC_COL( )
-	-	GMAC_CRS( )

2.3 USB

USB[1:0]_XI USB[1:0]_XO	I/O			VDD_3V3_USB	
USB[1:0]_TXRTUNE	A			VDD_3V3_USB	
USB[1:0]_DP	I/O	'h0		VDD_3V3_USB	
USB[1:0]_DM	I/O	'h0		VDD_3V3_USB	
USB[1:0]_OVRCUR	I			VDD_3V3_USB	
OTG_XI OTG_XO	I			VDD_3V3_USB	
OTG_TXRTUNE	A			VDD_3V3_USB	
OTG_DP	I/O	'h0		VDD_3V3_USB	
OTG_DM	I/O	'h0		VDD_3V3_USB	
OTG_DRVBUS	O	'h0		VDD_3V3_USB	
OTG_ID	I			VDD_3V3_USB	
OTG_VBUS	A			VBUS_5V	

2.4 SPI

SPI[1:0]_CLK	O	'h0		VDD_3V3		
SPI[1:0]_CSN	O	'hx		VDD_3V3		
SPI[1:0]_MOSI	O	'hx		VDD_3V3		
SPI[1:0]_MISO	I			VDD_3V3		
PRT_SPI_CLK	O	'h0		VDD_3V3		

PRT_SPI_CSN	O	'hx		VDD_3V3		
PRT_SPI_MOSI	O	'hx		VDD_3V3		
PRT_SPI_MISO	I			VDD_3V3		
SCA_SPI_CLK	O	'h0		VDD_3V3		
SCA_SPI_CSN	O	'hx		VDD_3V3		
SCA_SPI_MOSI	O	'hx		VDD_3V3		
SCA_SPI_MISO	I			VDD_3V3		

2.5 UART

UART[1:0]_TXD	O	'h1		VDD_3V3		
UART[1:0]_RXD	I			VDD_3V3		
PRT_UART_TXD	O	'h1		VDD_3V3		
PRT_UART_RXD	I			VDD_3V3		
SCA_UART_TXD	O	'h1		VDD_3V3		
SCA_UART_RXD	I			VDD_3V3		

2P0500 (UART0)

(UART1) UART0 2x4 4x2

UART

UART1 1x4 2x2

2.6 I²C

I2C[1:0]_SCL	O	’hx		VDD_3V3		
I2C[1:0]_SDA	I/O	’hx		VDD_3V3		
PRT_I2C[1:0]_SCL	O	’hx		VDD_3V3		
PRT_I2C[1:0]_SDA	I/O	’hx		VDD_3V3		

2.7 PRINTER

PRT_VIDOUT[15:0]	O	’hx		VDD_3V3		

TTL LVDS

	PRT_VIDOUT[0]	PRT_VIDOUT0
	PRT_VIDOUT[1]	PRT_VIDOUT1
	PRT_VIDOUT[2]	PRT_VIDOUT2
	PRT_VIDOUT[3]	PRT_VIDOUT3
	PRT_VIDOUT[4]	PRT_VIDOUT4
	PRT_VIDOUT[5]	PRT_VIDOUT5
	PRT_VIDOUT[6]	PRT_VIDOUT6
	PRT_VIDOUT[7]	PRT_VIDOUT7

LVDS LVDS

	PRT_VIDOUT[0]	
	PRT_VIDOUT[1]	
	PRT_VIDOUT[2]	
	PRT_VIDOUT[3]	
	PRT_VIDOUT[4]	
	PRT_VIDOUT[5]	
	PRT_VIDOUT[6]	
	PRT_VIDOUT[7]	
	PRT_VIDOUT[8]	
	PRT_VIDOUT[9]	
	PRT_VIDOUT[10]	
	PRT_VIDOUT[11]	
	PRT_VIDOUT[12]	
	PRT_VIDOUT[13]	
	PRT_VIDOUT[14]	
	PRT_VIDOUT[15]	

2.13

VDD_CORE	P		1.15V
VDD_1V1_USB	P		1.15V
VDD_NODE_PLL	P		1.15V/1.2V
VDD_DDR_PLL	P		1.15V/1.2V
VDD_SOC_PLL	P		1.15V/1.2V
VDDIO_DDR	P		1.5V
DDR_VREF	P		0.75V
VDD_3V3	P		3.3V
VDD_3V3_USB	P		3.3V
VDD_RTC	P		2.7V
VDD_3V3_DAC	P		3.3V
VDD_3V3_LVDS	P		3.3V
VDD_3V3_THSENS	P		3.3V
VSS	G		0V
VSS_RTC	G		0V
VSS_DAC	G		0V
VSS_LVDS	G		0V
VSS_NODE_PLL	G		0V
VSS_DDR_PLL	G		0V
VSS_SOC_PLL	G		0V

2.14

DOTESTn	I			RTC_VDD	

2.15 JTAG

JTAG_SEL	I		IO_3V3	
JTAG_TCK	I		IO_3V3	
JTAG_TDI	I		IO_3V3	
JTAG_TMS	I		IO_3V3	
JTAG_TRST	I		IO_3V3	
JTAG_TDO	O	’h1	IO	

2.16

2- 2

prt_uart0_rx	pm0io[0]	prt_pwm[0]	PRT_GPIO00
prt_uart0_tx	pm0io[1]	prt_pwm[1]	PRT_GPIO01
prt_i2c0_scl	pm0io[2]	prt_pwm[2]	PRT_GPIO02
prt_i2c0_sda	pm0io[3]	prt_pwm[3]	PRT_GPIO03
prt_i2c1_scl	prt_uart1_rx	prt_pwm[4]	PRT_GPIO04
prt_i2c1_sda	prt_uart1_tx	prt_pwm[5]	PRT_GPIO05
prt_spi_clk	gmac0_col	prt_pwm[6]	PRT_GPIO06
prt_spi_miso	gmac0_crs	prt_pwm[7]	PRT_GPIO07
prt_spi_mosi	gmac0_ptp_trig	prt_pwm[8]	PRT_GPIO08
prt_spi_cs	gmac0_ptp_pps	prt_pwm[9]	PRT_GPIO09
pm0io[0]	prt_vid_out[16]	prt_pwm[10]	PRT_GPIO10
pm0io[1]	prt_vid_out[17]	prt_pwm[11]	PRT_GPIO11
pm0io[2]	prt_vid_out[18]	prt_pwm[12]	PRT_GPIO12
pm0io[3]	prt_vid_out[19]	prt_pwm[13]	PRT_GPIO13
pm0io[4]	prt_vid_out[20]	prt_pwm[14]	PRT_GPIO14
pm0io[5]	prt_vid_out[21]	prt_pwm[15]	PRT_GPIO15
pm0io[6]	prt_vid_out[22]	prt_pwm[16]	PRT_GPIO16
pm0io[7]	prt_vid_out[23]	prt_pwm[17]	PRT_GPIO17
pm0io[8]	prt_pwm[0]	vid_clk[0]	PRT_GPIO18
pm0io[9]	prt_pwm[1]	vid_clk[1]	PRT_GPIO19
pm0io[10]	prt_pwm[2]	vid_clk[2]	PRT_GPIO20
pm0io[11]	prt_pwm[3]	vid_clk[3]	PRT_GPIO21
pm0io[12]	prt_pwm[4]	prt_vid_en[0]	PRT_GPIO22
pm0io[13]	prt_pwm[5]	prt_vid_en[1]	PRT_GPIO23
pm0io[14]	prt_pwm[6]	prt_vid_en[2]	PRT_GPIO24
pm0io[15]	prt_pwm[7]	prt_vid_en[3]	PRT_GPIO25
pm0io[16]	prt_pwm[8]	prt_ovlin[0]	PRT_GPIO26
pm0io[17]	prt_pwm[9]	prt_ovlin[1]	PRT_GPIO27
pm0io[18]	prt_pwm[10]	prt_ovlin[2]	PRT_GPIO28
pm0io[19]	prt_pwm[11]	prt_ovlin[3]	PRT_GPIO29
pm0io[20]	prt_pwm[12]	prt_ovlin[4]	PRT_GPIO30
pm0io[21]	prt_pwm[13]	prt_ovlin[5]	PRT_GPIO31
pm0io[22]	prt_pwm[14]	prt_ovlin[6]	PRT_GPIO32
pm0io[23]	prt_pwm[15]	prt_ovlin[7]	PRT_GPIO33
pm0io[24]	prt_vid_out[24]	prt_ovlin[8]	PRT_GPIO34
pm0io[25]	prt_vid_out[25]	prt_ovlin[9]	PRT_GPIO35
pm0io[26]	prt_vid_out[26]	prt_ovlin[10]	PRT_GPIO36
pm0io[27]	prt_vid_out[27]	prt_ovlin[11]	PRT_GPIO37
pm0io[28]	prt_vid_out[28]	prt_ovlin[12]	PRT_GPIO38
pm0io[29]	prt_vid_out[29]	prt_ovlin[13]	PRT_GPIO39
pm0io[30]	prt_vid_out[30]	prt_ovlin[14]	PRT_GPIO40
pm0io[31]	prt_vid_out[31]	prt_ovlin[15]	PRT_GPIO41
prt_vid_out[0]	pm0io[8]	pm0io[16]	PRT_GPIO42
prt_vid_out[1]	pm0io[9]	pm0io[17]	PRT_GPIO43
prt_vid_out[2]	pm0io[10]	pm0io[18]	PRT_GPIO44
prt_vid_out[3]	pm0io[11]	pm0io[19]	PRT_GPIO45
prt_vid_out[4]	pm0io[12]	pm0io[20]	PRT_GPIO46

sca_cisclk[2]	pm0io[28]	pm1io[28]	SCA_GPIO34
sca_cispls[0]	pm0io[29]	pm1io[29]	SCA_GPIO35
sca_cispwm	pm0io[30]	pm1io[30]	SCA_GPIO36

3

3.1 DDR3

2P0500

3.1.1 DDR3

133-400MHZ

3.1.2 DDR3

2P0500 1 CS 19 16
3 Bank
DDR3
CS_n 1 RAS_n 16
CAS_n 16 BANK_n 3
CPU

slave

Open Page/Close Page

2P0500

DCC

133-400MHZ

32/16 16 16

3.2 USB

2P0500 USB

USB Rev 1.1 USB Rev 2.0

OHCI Rev 1.0 EHCI Rev 1.0

LS Low Speed FS Full Speed HS High Speed USB

USB2.0

USB2.0 EHCI

OHCI EHCI

OHCI

EHCI

3.3 OTG

2P0500 OTG :

HNP SRP

DMA OTG

device 480Mbps

host 480Mbps

device 10 endpoint endpoint0

device 4 IN

host 12 channel channel

host periodic OUT

3.4 GMAC

2P0500 GMAC GMAC0 GMAC1

3.5 SPI

SPI

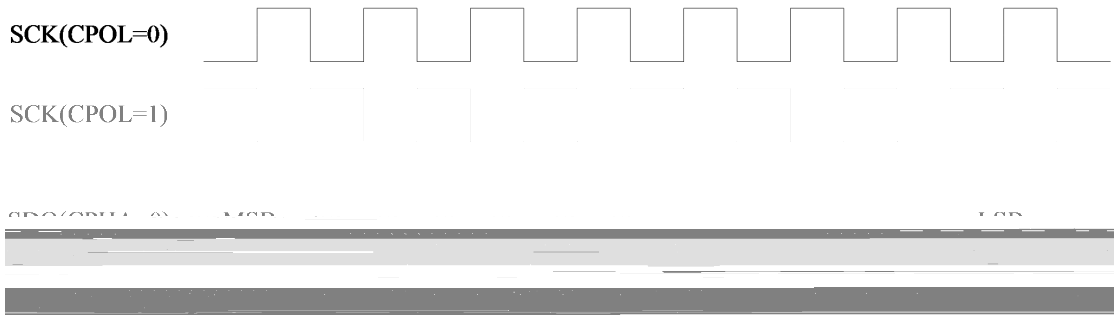
2P0500 SPI

SPI IO SPI Flash

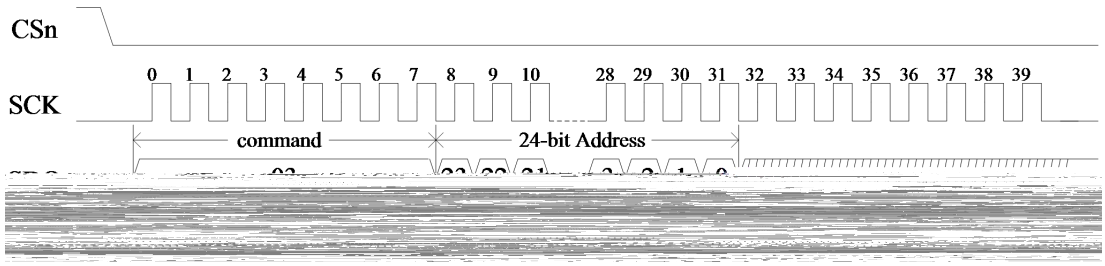
memory memory BOOT

SPI Flash

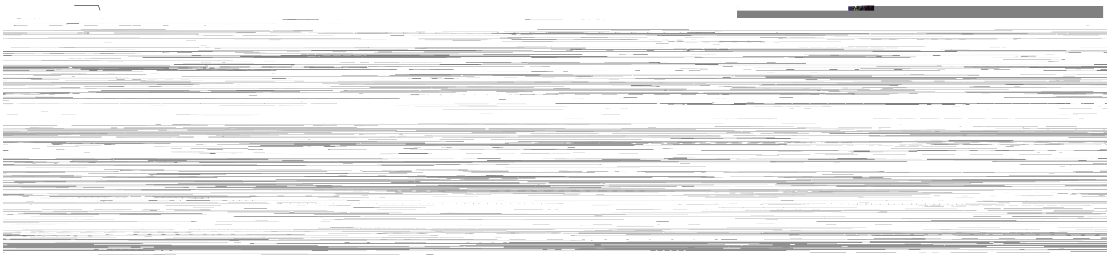
SPI



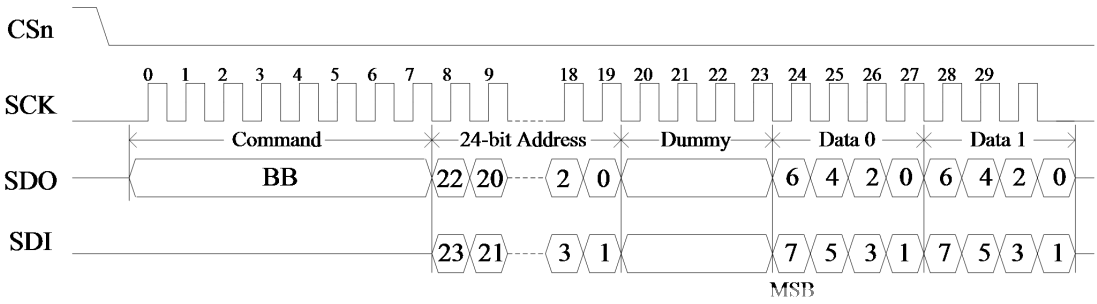
3.1 SPI



3.2 SPI Flash



3.3 SPI Flash



3.4 SPI Flash I/O

3.6 UART

2P0500 8 UART 1 (UART0) 1 (UART1) 2 2 (UART2/UART3) 1 4 2 (UART0 UART1 UART2 UART3 UART0) 1 2 2 (UART1 UART3 UART1) APB

UART MODEM RS232 16550A

3.7 I²C

2P0500 I2C

I2C SDA SCL

400kbps

3.8 PRINTER

2P0500 JBIG85 8

3.9 SCANNER

2P0500 RGB segment

CIS AFE

3.10 DA

2P0500 DA 4 8 DA

3.11 SDIO

2P0500 SDIO/eMMC SD/eMMC Memory SDIO

SDIO0 SD/eMMC Memory

SDIO

(512K Byte

)

3.12 PMIO

2P0500 IO Programmable Multifunction IO PMIO PMIO

PMIO PMIO Timer PWM Generator GPIO

3.13 PWM

2P0500 40 / PWM PWM PWM 32

3.14 GPIO

2P0500 139 GPIO

GPIO

3.15 HPET

2P0500 32 1 2

3.16 RTC

RTC

RTC 10

RTC 32.768KHZ

0.1

3.17

2P0500

(OTG)

Dynamic Power Management DPM

NODE CORE+SCACHE DDR IMAGE SCAN SYS

Dynamic Frequency Scaling DFS DFS

LA132

3

4

4.1

4.2

5

5.1

5.1.1

VDD_1V1_USB	USB vp vptx	-0.3	1.21	V
VDD_3V3_USB	USB vph	-0.3	3.47	V
VDD_3V3_DAC	DA	-0.3	3.47	V
VDD_3V3_LVDS	LVDS	-0.3	3.47	V
VDD_3V3_THSENS	THSNES	-0.3	3.47	V
VDD_PLL	PLL	-0.3	1.3	V
ESD		-	2000	V
Tstg		-55	125	

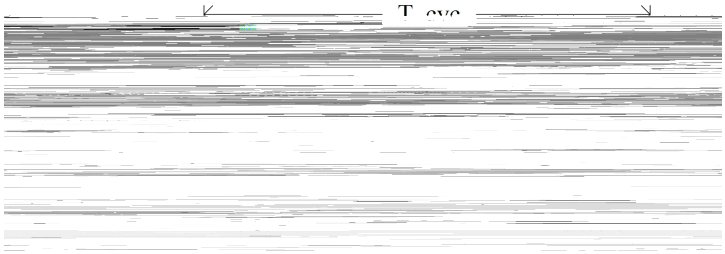
5.1.3

5- 3

	(25)	**(W)**
	CPU 750MHz; DDR 400MHz USB GMAC SPEC CPU2000	1.6W

5.2

5.2.1



5.1

SYS_CLK	Vih		2.0	-	V
	Vil		-	0.8	V
	T_cyc		9.99	10.01	ns
	T_hi		40%T_cyc	60%T_cyc	ns
	T_low		40%T_cyc	60%T_cyc	ns

5.3 DDR3

5.3.1

5- 4

Symbol	Parameter	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage	1.42	1.5	1.58	V
V_{DDQ}	Supply Voltage for Output	1.42	1.5	1.58	V

5.3.2

5.3.2.1

5- 5

Symbol	Parameter	DDR3-800/1066/1333/1600		Unit
		Min	Max	
VIH.CA(DC100)	DC input logic high	Vref + 0.100	VDD	V
VIL.CA(DC100)	DC input logic low	VSS	Vref - 0.100	V
VIH.CA(AC175)	AC input logic high	Vref + 0.175	Note 2	V
VIL.CA(AC175)	AC input logic low	Note 2	Vref - 0.175	V
VIH.CA(AC150)	AC input logic high	Vref + 0.150	Note 2	V
VIL.CA(AC150)	AC input logic low	Note 2	Vref - 0.150	V
$V_{RefCA(DC)}$	Reference Voltage for ADD, CMD inputs	0.49 * VDD	0.51 * VDD	V

5- 6 DQ DM

Symbol	Parameter	DDR3-800, DDR3-1066		DDR3-1333, DDR3-1600		Unit
		Min	Max	Min	Max	
VIH.DQ(DC100)	DC input logic high	Vref + 0.100	VDD	Vref + 0.100	VDD	V
VIL.DQ(DC100)	DC input logic low	VSS	Vref - 0.100	VSS	Vref - 0.100	V
VIH.DQ(AC175)	AC input logic high	Vref + 0.175	-	-	-	V
VIL.DQ(AC175)	AC input logic low	-	Vref - 0.175	-	-	V
VIH.DQ(AC150)	AC input logic high	Vref + 0.150	-	Vref + 0.150	-	V
VIL.DQ(AC150)	AC input logic low	-	Vref - 0.150	-	Vref - 0.150	V
$V_{RefDQ(DC)}$	Reference Voltage for DQ, DM inputs	0.49 * VDD	0.51 * VDD	0.49 * VDD	0.51 * VDD	V

5.3.2.2

5.3 ac-swing ac-level tDVA

5- 7

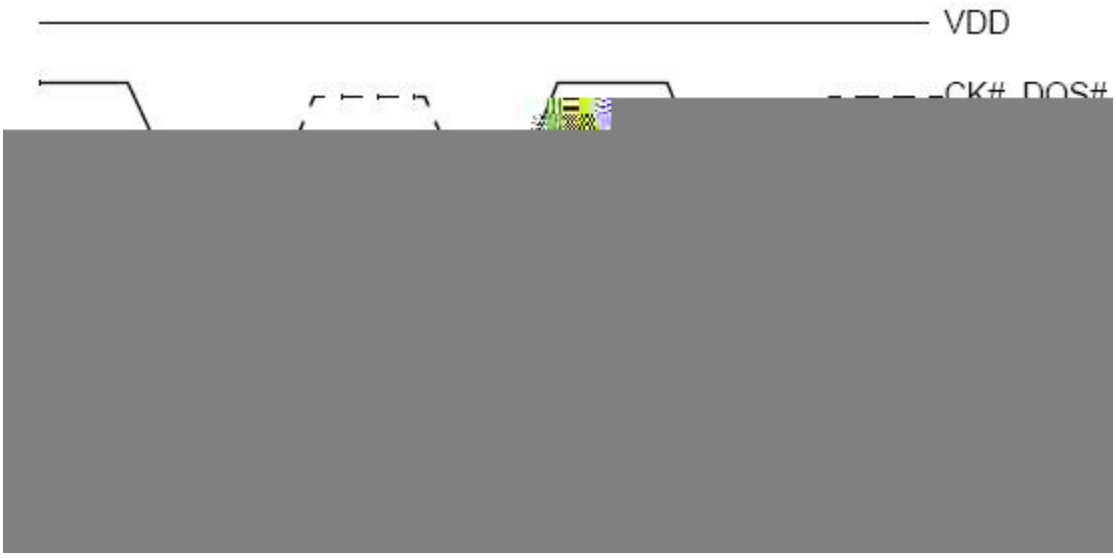
Symbol	Parameter	DDR3-800,1066		Unit
		Min	Max	
V_{IHdiff}	Differential input high	+ 0.200	note 3	V
V_{ILdiff}	Differential input logic low	Note 3	- 0.200	V
$V_{IHdiff(ac)}$	Differential input high ac	2 x (VIH(ac) - Vref)	Note 3	V
$V_{ILdiff(ac)}$	Differential input low ac	note 3	2 x (VIL(ac) - Vref)	V

5.3.2.3

CK CK DQS DQS 5- 8

VIX

VDD VSS



5.4 Vix

5- 8 (CK, DQS)

Symbol	Parameter	DDR3-800, DDR3-1066, DDR3-1333, DDR3-1600		Unit
		Min.	Max.	
VIX	Differential Input Cross Point Voltage relative to VDD/2 for CK,CK#	-150	150	mV
		-175	175	mV
VIX	Differential Input Cross Point Voltage relative to VDD/2 for DQS, DQS#	-150	150	mV

5.3.3

5.3.3.1

5- 9

Symbol	Parameter	DDR3-800, 1066, 1333, and 1600	Unit
VOH(DC)	DC output high measurement level (for IV curve linearity)	0.8 x VDDQ	V
VOM(DC)	DC output mid measurement level (for IV curve linearity)	0.5 x VDDQ	V
VOL(DC)	DC output low measurement level (for IV curve linearity)	0.2 x VDDQ	V
VOH(AC)	AC output high measurement level (for output SR)	VTT + 0.1 x VDDQ	V
VOL(AC)	AC output low measurement level (for output SR)	VTT - 0.1 x VDDQ	V

5.3.3.2

5- 10

Symbol	Parameter	DDR3-800, 1066, 1333, and 1600	Unit
VOHdiff(AC)	AC differential output high measurement level (for output SR)	+ 0.2 x VDDQ	V
VOLdiff(AC)	AC differential output low measurement level (for output SR)	- 0.2 x VDDQ	V

5.3.3.3

VOL AC VOH AC 5-11 5.4

5-11

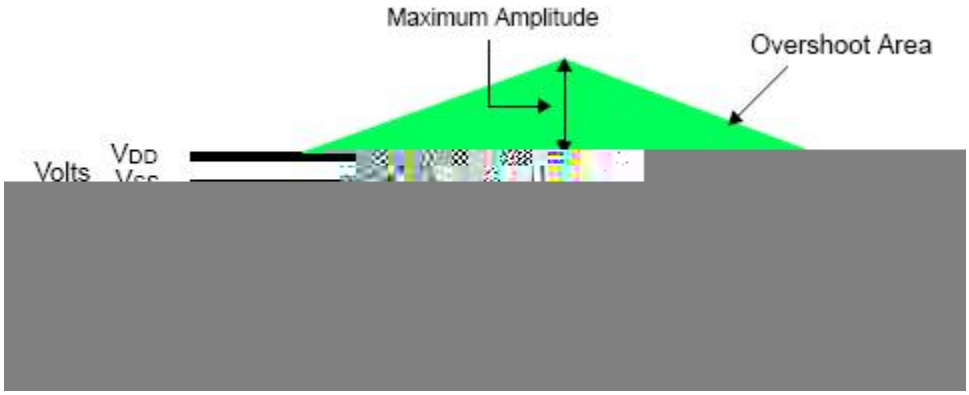
Description	Measured from	Measured to	Defined by
Single-ended output slew rate for rising edge	VOL(AC)	VOH(AC)	[VOH(AC) -VOL(AC)] / Îeq

5.6

5- 14

		DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		Units
Parameter	**Symbol**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	**Min**	**Max**	
Differential Output Slew Rate	SRQdiff	5	10	5	10	5	10	TBD	10	V/ns

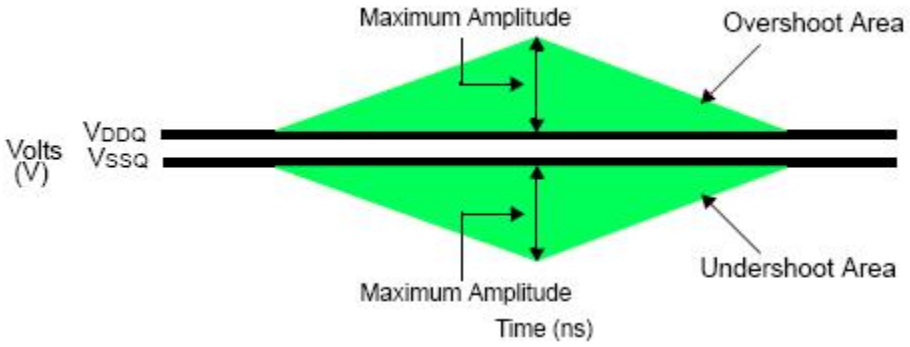
5.3.3.5



5.7

5- 16 /

	DDR3-800	DDR3-1066	DDR3-1333	DDR3-1600	Units
Maximum peak amplitude allowed for overshoot area.	0.4	0.4	0.4	0.4	V
Maximum peak amplitude allowed for undershoot area.	0.4	0.4	0.4	0.4	V
Maximum overshoot area above VDDQ	0.25	0.19	0.15	0.13	V-ns
Maximum undershoot area below VSSQ	0.25	0.19	0.15	0.13	V-ns
(CK, CK#, DQ, DQS, DQS#, DM)					



5.8

5.3.3.6 ODT

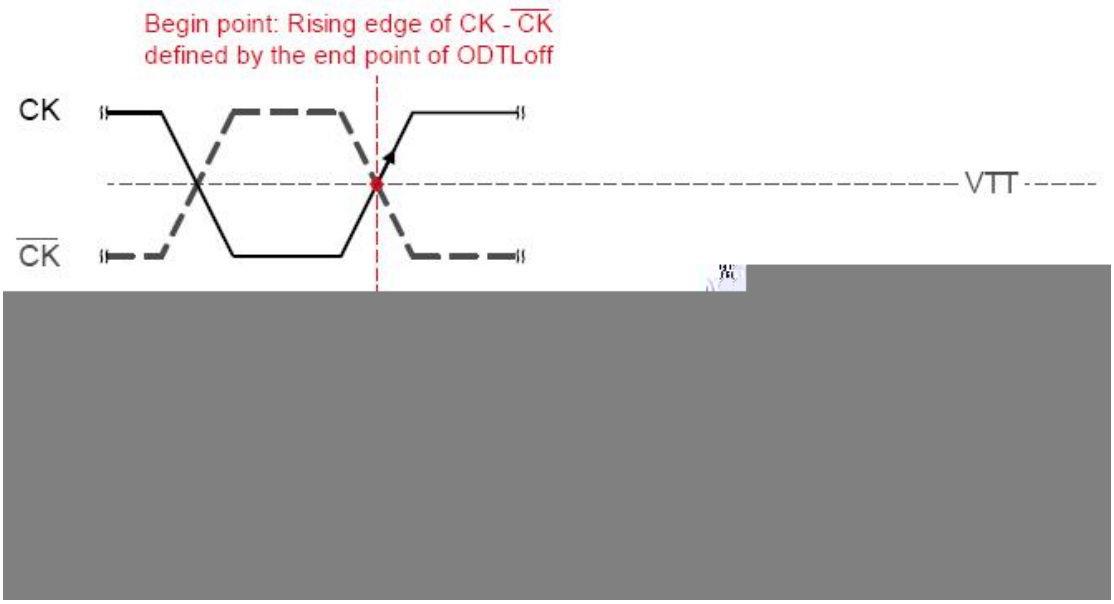
5- 17 ODT

Symbol	Begin Point Definition	End Point Definition	Figure
tAON	Rising edge of CK -CK# defined by the end point of ODTLon	Extrapolated point at VSSQ	Figure 103
tAONPD	Rising edge of CK -CK# with ODT being first registered high	Extrapolated point at VSSQ	Figure 104
tAOF	Rising edge of CK -CK#defined by the end point of ODTLoff	End point: Extrapolated point at VRTT_Nom	Figure 105
tAOFPD	Rising edge of CK -CK# with ODT being first registered low	End point: Extrapolated point at VRTT_Nom	Figure 106
tADC	Rising edge of CK -CK# defined by the end point of ODTLcnw, ODTLcwn4 or ODTLcwn8	End point: Extrapolated point at VRTT_Wr and VRTT_Nom respectively	Figure 107

5- 18 ODT

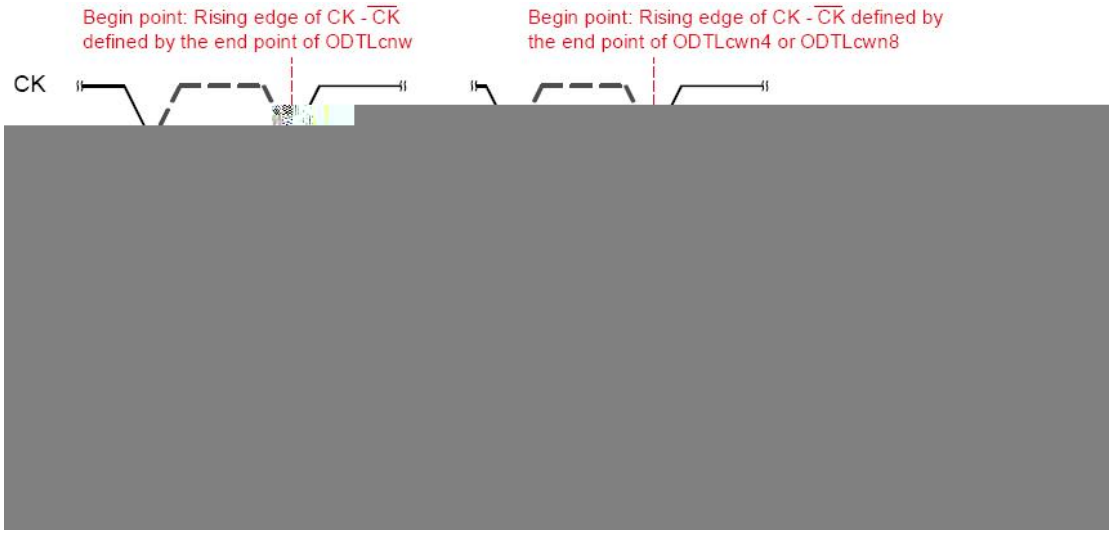
Measured Parameter	RTT_Nom Setting	RTT_Wr Setting	VSW1[V]	VSW2[V]
tAON	RZQ/4	NA	0.05	0.10
	RZQ/12	NA	0.10	0.20
tAONPD	RZQ/4	NA	0.05	0.10
	RZQ/12	NA	0.10	0.20
tAOF	RZQ/4	NA	0.05	0.10
	RZQ/12	NA	0.10	0.20
tAOFPD	RZQ/4	NA	0.05	0.10
	RZQ/12	NA	0.10	0.20
tAD	RZQ/12	RZQ/2	0.20	0.30

5.10 tAONPD



5.11 tAOF

5.12 tAOFPD



5.13 tADC

5.3.4 IDD IDDQ

5- 19 IDD IDDQ

Symbol	DDR3-800		DDR3-1066			DDR3-1333				DDR3-1600				Unit
	5-5-5	6-6-6	6-6-6	7-7-7	8-8-8	7-7-7	8-8-8	9-9-9	10-10-10	8-8-8	9-9-9	10-10-10	11-11-11	
tCK	2.5		1.875			1.5				1.25				ns
CL	5	6	6	7	8	7	8	9	10	8	9	10	11	nCK
nRCD	5	6	6	7	8	7	8	9	10	8	9	10	11	nCK
nRC	20	21	26	27	28	31	32	33	34	36	37	38	39	nCK
nRAS	15		20			24				28				n= î

5.3.5 /

5- 20 /

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Input/output capacitance (DQ, DM, DQS, DQS#, TDQS,TDQS#)	CIO	1.5	3.0	1.5	2.7	1.5	2.5	1.5	2.3	pF
Input capacitance, CK and CK#	CCK	0.8	1.6	0.8	1.6	0.8	1.4	0.8	1.4	pF
Input capacitance delta, CK and CK#	CD ·,									

5- 23 DDR3-1066 Speed Bins and Operating Conditions

Speed Bin			DDR3-1066E		DDR3-1066F		DDR3-1066G		
CL - nRCD – nRP			6-6-6		7-7-7		8-8-8		Unit
Parameter		Symbol	Min.	Max.	Min.	Max.	Min.	Max.	
Internal read command to first data		tAA	11.25	20	13.125	20	15	20	ns
ACT to internal read or write delay time		tRCD	11.25		13.125		15		ns
PRE command period		tRP	11.25		13.125		15		ns
ACT to ACT or REF command period		tRC	48.75		50.625		52.5		ns
ACT to PRE command period		tRAS	37.5	9 * tREFI	37.5	9 * tREFI	37.5	9 * tREFI	ns
CL = 5	CWL = 5	tCK(AVG)	2.5	3.3	3.0	3.3	3.0	3.3	ns
	CWL = 6	tCK(AVG)	Reserved		Reserved		Reserved		ns
CL = 6	CWL = 5	tCK(AVG)	2.5	3.3	2.5	3.3	2.5	3.3	

5- - - - -

5- 25 DDR3-1600 Speed Bins and Operating Conditions

SpeedBin	DDR3-1600G (optional)	DDR3-1600H	DDR3-1600J	DDR3-1600K

5.3.8 DDR3

5- 26 Timing Parameters by Speed Bin

Parameter	Symbol	DDR3-800		DDR3-1066		DDR3-1333		DDR3-1600		Units
		Min	Max	Min	Max	Min	Max	Min	Max	
Clock Timing										
Minimum Clock Cycle Time (DLL off mode)	tCK(DLL_OFF)	8	-	8	-	8	-	8	-	ns
Average Clock Period	tCK(avg)									ps
Average high pulse width	tCH(avg)	0.47	0.53	0.47	0.53	0.47	0.53	0.47	0.53	tCK(avg)
Average low pulse width	tCL(avg)	0.47	0.53	0.47	0.53	0.47	0.53	0.47	0.53	tCK(avg)
Absolute Clock Period	tCK(abs)	tCK(avg) min + tJIT(per)min	tCK(avg) max + tJIT(per) max	tCK(avg) min + tJIT(per)min	tCK(avg) max + tJIT(per) max	tCK(avg)min + tJIT(per) min	tCK(avg) max + tJIT(per) max	tCK(avg)min + tJIT(per) min	tCK(avg) max + tJIT(per) max	ps
Absolute clock HIGH pulse width	tCH(abs)	0.43	-	0.43	-	0.43	-	0.43	-	tCK(avg)
Absolute clock LOW pulse width	tCL(abs)	0.43	-	0.43	-	0.43	-	0.43	-	tCK(avg)
Clock Period Jitter	JIT(per)	-100	100	-90	90	-80	80	-70	70	ps
Clock Period Jitter during DLL locking period	tJIT(per,lck)	-90	90	-80	80	-70	70	-60	60	ps
Cycle to Cycle Period Jitter	tJIT(cc)	200		180		160		140		ps
Cycle to Cycle Period Jitter during DLL locking period	tJIT(cc,lck)	180		160		140		120		ps
Duty Cycle Jitter	tJIT(duty)	-	-	-	-	-	-	-	-	ps
Cumulative error across 2 cycles	tERR(2per)	-147	147	-132	132	-118	118	-103	103	ps
Cumulative error across 3 cycles	tERR(3per)	-175	175	-157	157	-140	140	-122	122	ps
Cumulative error across 4 cycles	tERR(4per)	-194	194	-175	175	-155	155	-136	136	ps
Cumulative error across 5 cycles	tERR(5per)	-209	209	-188	188	-168	168	-147	147	ps
Cumulative error across 6 cycles	tERR(6per)	-222	222	-200	200	-177	177	-155	155	ps
Cumulative error across 7 cycles	tERR(7per)	-232	232	-209	209	-186	186	-163	163	ps
Cumulative error across 8 cycles	tERR(8per)	-241	241	-217	217	-193	193	-169	169	ps
Cumulative error across 9 cycles	tERR(9per)	-249	249	-224	224	-200	200	-175	175	ps

Cumulative error across 10 cycles	tERR(10per)	-257	257	-231	231	-205	205	-180	180	ps
Cumulative error across 11 cycles	tERR(11per)	-263	263	-237	237	-210	210	-184	184	ps
Cumulative error across 12 cycles	tERR(12per)	-269	269	-242	242	-215	215	-188	188	ps
Cumulative error across n = 13, 14 . . . 49, 50 cycles	tERR(nper)	tERR(nper)min = (1 + 0.68ln(n)) * tJIT(per)min tERR(nper)max = (1 + 0.68ln(n)) * tJIT(per)max	ps	24						
Data Timing										
DQS, DQS# to DQ skew, per group, per access	tDQSQ	-	200	-	150	-	125	-	100	ps
DQ output hold time from DQS, DQS#	tQH	0.38	-	0.38	-	0.38	-	0.38	-	tCK(avg)
DQ low-impedance time from CK, CK#	tLZ(DQ)	-800	400	-600	300	-500	250	-450	225	ps
DQ high impedance time from CK, CK#	tHZ(DQ)	-	400	-	300	-	250	-	225	ps
Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels	tDS(base)AC175	75		25		-		-		ps
Data setup time to DQS, DQS# referenced to Vih(ac) / Vil(ac) levels	tDS(base)AC150	125		75		30		10		ps
Data hold time from DQS, DQS# referenced to Vih(dc) / Vil(dc) levels	tDH(base)DC100	150		100		65		45		ps
DQ and DM Input pulse width for each input	tDIPW	600	-	490	-	400	-	360	-	ps
Data Strobe Timing										
DQS,DQS# differential READ Preamble	tRPRE	0.9	Note19	0.9	Note19	0.9	Note19	0.9	Note19	tCK(avg)
DQS, DQS# differential READ Postamble	tRPST	0.3	Note11	0.3	Note11	0.3	Note11	0.3	Note11	tCK(avg)

DQS, DQS# differential output high time	tQSH	0.38	-	0.38	-	0.40	-	0.40	-	tCK(avg)
DQS, DQS# differential output low time	tQSL	0.38	-	0.38	-	0.40	-	0.40	-	tCK(avg)
DQS, DQS# differential WRITE Preamble	tWPRE	0.9	-	0.9	-	0.9	-	0.9	-	tCK(avg)
DQS, DQS# differential WRITE Postamble	tWPST	0.3	-	0.3	-	0.3	-	0.3	-	tCK(avg)
DQS, DQS# rising edge output access time from rising CK, CK#	tDQSCK	-400	400	-300	300	-255	255	-225	225	ps
DQS and DQS# low-impedance time (Referenced from RL - 1)	tLZ(DQS)	-800	400	-600	300	-500	250	-450	225	ps
DQS and DQS# high-impedance time (Referenced from RL + BL/2)	tHZ(DQS)	-	400	-	300	-	250	-	225	ps
DQS, DQS# differential input low pulse width	tDQSL	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK(avg)
DQS, DQS# differential input high pulse width	tDQSH	0.45	0.55	0.45	0.55	0.45	0.55	0.45	0.55	tCK(avg)
DQS, DQS# rising edge to CK, CK# rising edge	tDQSS	-0.25	0.25	-0.25	0.25	-0.25	0.25	-0.27	0.27	tCK(avg)
DQS, DQS# falling edge setup time to CK, CK# rising edge	tDSS	0.2	-	0.2	-	0.2	-	0.18	-	tCK(avg)
DQS, DQS# falling edge hold time from CK, CK# rising edge	tDSH	0.2	-	0.2	-	0.2	-	0.18	-	tCK(avg)
Command and Address Timing										
DLL locking time	tDLLK	512	-	512	-	512	-	512	-	nCK
Internal READ Command to PRECHARGE Command delay	tRTP	max(4nCK, 7.5ns)		max(4nCK,7.5ns)	-	max(4nCK,7.5ns)	-	max(4nCK,7.5ns)	-	
Delay from start of internal write transaction to internal read command	tWTR	max(4nCK, 7.5ns)		max(4nCK,7.5ns)	-	max(4nCK,7.5ns)	-	max(4nCK,7.5ns)	-	
WRITE recovery time	tWR	15		15	-	15	-	15	-	ns
Mode Register Set command cycle time	tMRD	4		4	-	4	-	4	-	nCK

Mode Register
Set command
update delay

Power-up and RESET calibration time	tZQinit	max(512nCK,640ns)	-	max(512nCK,640ns)	-	max(512nCK,640ns)	-	max(512nCK,640ns)	-	
Normal operation Full calibration time	tZQoper	max(256nCK,320ns)	-	max(256nCK,320ns)	-	max(256nCK,320ns)	-	max(256nCK,320ns)	-	
Normal operation Short calibration time	tZQCS	max(64nCK,80ns)	-	max(64nCK,80ns)	-	max(64nCK,80ns)	-	max(64nCK,80ns)	-	
Reset Timing										
Exit Reset from CKE HIGH to a valid command	tXPR	max(5nCK,tRFC(min)+10ns)	-	max(5nCK,tRFC(min)+10ns)	-	max(5nCK,tRFC(min)+10ns)	-	max(5nCK,tRFC(min)+10ns)	-	
Self Refresh Timings										
Exit Self Refresh to commands not requiring a locked DLL	tXS	max(5nCK, tRFC(min) + 10ns)	-	max(5nCK, tRFC(min) + 10ns)	-	max(5nCK, tRFC(min) + 10ns)	-	max(5nCK, tRFC(min) + 10ns)	-	
Exit Self Refresh to commands requiring a locked DLL	tXSDLL	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	tDLLK(min)	-	nCK
Minimum CKE low width for Self Refresh entry to exit timing	tCKESR	tCKE(min) + 1 nCK	-	tCKE(min) + 1 nCK	-	tCKE(min) + 1 nCK	-	tCKE(min) + 1 nCK	-	
Valid Clock Requirement after Self Refresh Entry (SRE) or Power-Down Entry (PDE)	tCKSRE	max(5nCK,10ns)	-	max(5nCK,10ns)	-	max(5nCK,10ns)	-	max(5nCK,10ns)	-	
Valid Clock Requirement before Self Refresh Exit (SRX) or Power-Down Exit (PDX) or Reset Exit	tCKSRX	max(5nCK,10ns)	-	max(5nCK,10ns)	-	max(5nCK,10ns)	-	max(5nCK,10ns)	-	
Power Down Timings										
Exit Power Down with DLL on to any valid command; Exit Precharge Power Down with DLL frozen to commands not requiring a locked DLL	tXP	max(3nCK,7.5ns)	-	max(3nCK,7.5ns)	-	max(3nCK,6ns)	-	max(3nCK,6ns)	-	
Exit Precharge Power Down with DLL frozen to commands requiring a locked DLL	tXPDLL	max(10nCK,24ns)	-	max(10nCK,24ns)	-	max(10nCK,24ns)	-	max(10nCK,24ns)	-	

CKE minimum pulse width	tCKE	max(3nCK 7.5ns)	-	max(3nCK ,5.625ns)	-	max(3nCK,5.625ns)	-	max(3nCK,5ns)	-	
Command pass disable delay	tCPDED	1	-	1	-	1	-	1	-	nCK
Power Down Entry to Exit Timing	tPD	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	tCKE(min)	9*tREFI	
Timing of ACT command to Power Down entry	tACTPDEN	1	-	1	-	1	-	1	-	nCK
Timing of PRE or PREA command to Power Down entry	tPRPDEN	1	-	1	-	1	-	1	-	nCK
Timing of RD/RDA command to Power Down entry	tRDPDEN	RL+4+1	-	RL+4+1	-	RL+4+1	-	RL+4+1	-	nCK
Timing of WR command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRPDEN	WL+4+(tWR/tCK(avg))	-	WL+4+(tWR/tCK(avg))	-	WL+4+(tWR/tCK(avg))	-	WL+4+(tWR/tCK(avg))	-	nCK
Timing of WRA command to Power Down entry (BL8OTF, BL8MRS, BC4OTF)	tWRAPDEN	WL+4+WR+1	-	WL+4+WR+1	-	WL+4+WR+1	-	WL+4+WR+1	-	nCK
Timing of WR command to Power Down entry (BC4MRS)	tWRPDEN	WL+2+(tWR/tCK(avg))	-	WL+2+(tWR/tCK(avg))	-	WL+2+(tWR/tCK(avg))	-	WL+2+(tWR/tCK(avg))	-	nCK
Timing of WRA command to Power Down entry (BC4MRS)	tWRAPDEN	WL+2+WR+1	-	WL+2+WR+1	-	WL+2+WR+1	-	WL+2+WR+1	-	nCK
Timing of REF command to Power Down entry	tREFPDEN	1	-	1	-	1	-	1	-	nCK
Timing of MRS command to Power Down entry	tMRSPDEN	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-	tMOD(min)	-	
ODT Timings										
ODT turn on Latency	ODTLon	WL-2=CWL+AL-2								nCK
ODT turn off Latency	ODTLoff	WL-2=CWL+AL-2								nCK
ODT high time without write command or with write command and BC4	ODTH4	4	-	4	-	4	-	4	-	nCK
ODT high time with Write command and BL8	ODTH8	6	-	6	-	6	-	6	-	nCK

Asynchronous RTT turn-on delay (Power-Down with DLL frozen)	tAONPD	2	8.5	2	8.5	2	8.5	2	8.5	ns
Asynchronous RTT turn-off delay (Power-Down with DLL frozen)	tAOFPD	2	8.5	2	8.5	2	8.5	2	8.5	ns
RTT turn-on	tAON	-400	400	-300	300	-250	250	-225	225	ps
RTT_Nom and RTT_WR turn-off time from ODTLoff reference	tAOF	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	tCK(avg)
RTT dynamic change skew	tADC	0.3	0.7	0.3	0.7	0.3	0.7	0.3	0.7	tCK(avg)
Write Leveling Timings										
First DQS/DQS# rising edge after write leveling mode is programmed	tWLMRD	40	-	40	-	40	-	40	-	nCK
DQS/DQS# delay after write leveling mode is programmed	tWLDQSEN	25	-	25	-	25	-	25	-	nCK
Write leveling setup time from rising CK, CK# crossing to rising DQS, DQS# crossing	tWLS	325	-	245	-	195	-	165	-	ps
Write leveling hold time from rising DQS, DQS# crossing to rising CK, CK# crossing	tWLH	325	-	245	-	195	-	165	-	ps
Write leveling output delay	tWLO	0	9	0	9	0	9	0	7.5	ns
Write leveling output error	tWLOE	0	2	0	2	0	2	0	2	ns

5.4 RGMII

RGMII VDD_3V3 3.3V

5.4.1 RGMII

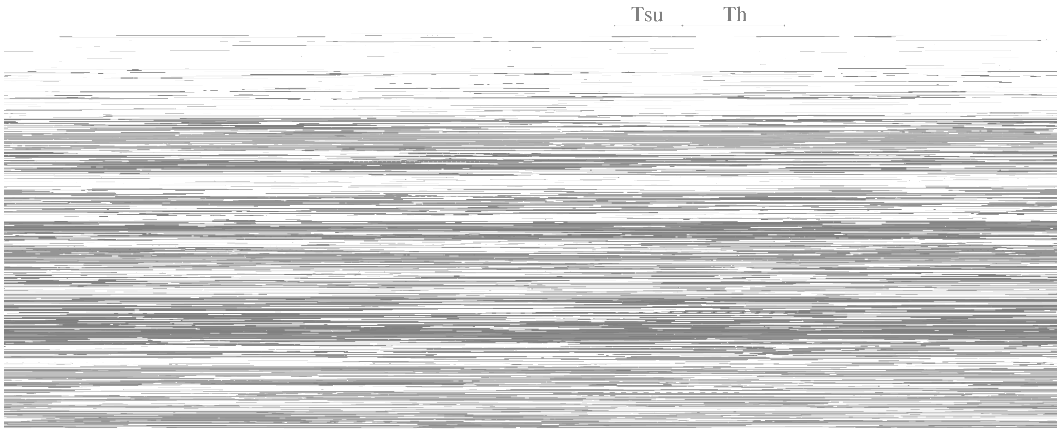
5-27 RGMII

Ioh	(VDDE-0.4V)	12	mA
Iol	(0.4V)	12	mA

5- 28 RGMII

Vih		3.3V	2.0	3.6	V
Vil		3.3V	-0.3	0.8	V

5.4.2 RGMII



5.14 RGMII

5- 29 RGMII

Tsu	RX	1	-	-	ns
Th	RX	1	-	-	ns
Tskew	TXCK TX	-500	-	+500	ps
Tr	TXD/TXCK (10pf)			1.2	ns
Tf	TXD/TXCK (10pf)			1.3	ns

5.5 USB

USB 2.0 7

5- 30 USB

Parameter	Symbol	Conditions	Min.	Max.	Units
InputLevelsforLow-/full-speed:					
High(driven)	VIH		2		V
High(floating)	VIHZ		2.7	3.6	V
Low	VIL			0.8	V
Differential Input Sensitivity	VDI	|(D+)-(D-)|	0.2		V
Differential Common Mode Range	VCM	Includes VDI range	0.8	2.5	V
Input Levels for High-speed:					
High-speed squelch detection threshold (differential signal amplitude)	VHSSQ		100	150	mV
High speed disconnect detection threshold (differential signal amplitude)	VHSDSC		525	625	mV
High-speed differential input signaling levels					
High-speed data signaling common mode voltage range(guide line for receiver)	VHSCM		-50	500	mV
Output Levels for Low-/full-speed:					
Low	VOL		0	0.3	V
High(Driven)	VOH		2.8	3.6	V
SE1	VOSE1		0.8		V
Output Signal Crossover Voltage	VCRS		1.3	2	V
Output Levels for High-speed:					
High-speed idle level	VHSOI		-10	10	mV
High-speed data signaling high	VHSOH		360	440	mV
High-speed data signaling low	VHSOL		-10	10	mV
Chirp J level(differential voltage)	VCHIRPJ		700	1100	mV
Chirp K level(differential voltage)	VCHIRPK		-900	-500	mV
Decoupling Capacitance:					
Downstream Facing Port Bypass Capacitance (perhub)	CHPB	VBUS to GND	120		F
Upstream Facing Port Bypass Capacitance	CRPB	VBUS to GND	1	10	F
Input Capacitance for Low-/full-speed:					
Downstream Facing Port	CIND			150	pF
Upstream Facing Port(w/ocable)	CINUB			100	pF
Transceiver edge rate control capacitance	CEDGE			75	pF
InputImpedanceforHigh-speed:					
TDRspecforhigh-speedtermination					

Terminations:					
Bus Pull-up Resistoron Upstream Facing Port	RPU	1.5k 5%	1.425	1.575	k
Bus Pull-down Resistoron Downstream Facing Port	RPD	15k 5%	14.25	15.75	k
Input impedance exclusive of pullup/pulldown(forlow-/full-speed)	ZINP		300		k
Termination voltage for upstream facing port pullup(RPU)	VTERM		3	3.6	V
Terminations in High-speed:					
Termination voltage in high-speed	VHSTERM		-10	10	mV

Parameter	Symbol	Conditions	Min.	Max.	Units
Driver Characteristics:					
Rise Time(10%-90%)	THSR		500		ps
Fall Time(10%-90%)	THSF		500		ps

5.6 SPI Flash

5- 34 SPI Flash

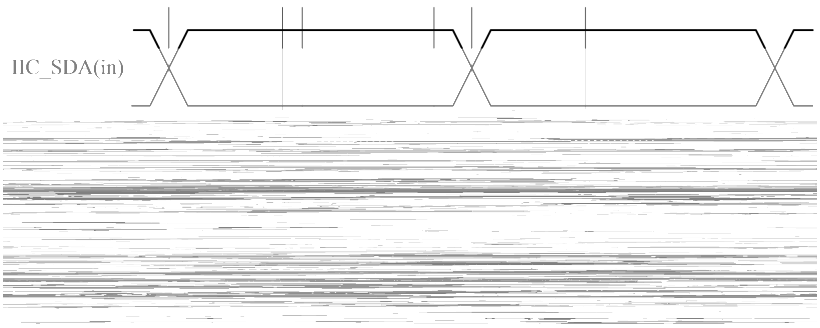
T_ckh	SCK	0.5T-1	-	-	ns
T_ckl	SCK	0.5T-1	-	-	ns
T_val	SCK	-5	-	5	ns
T_su		20	-	-	ns
T_h		0	-	-	ns

T SCK

5.7 I2C

5- 35 I2C

T_ckh	SCL	4	-	-	us
T_ckl	SCL	5	-	-	us
T_val	SCL	5	-	-	us
T_su	(SDA SCL)	0	-	-	us
T_h	(SCL SDA)	0	-	-	us



5.15 I2C

6

6.1

6- 1

Parameter	Value
TDP Max Power	5 Watts
Rth(J-C)	6 °C/W
Tj	125 °C

6.2

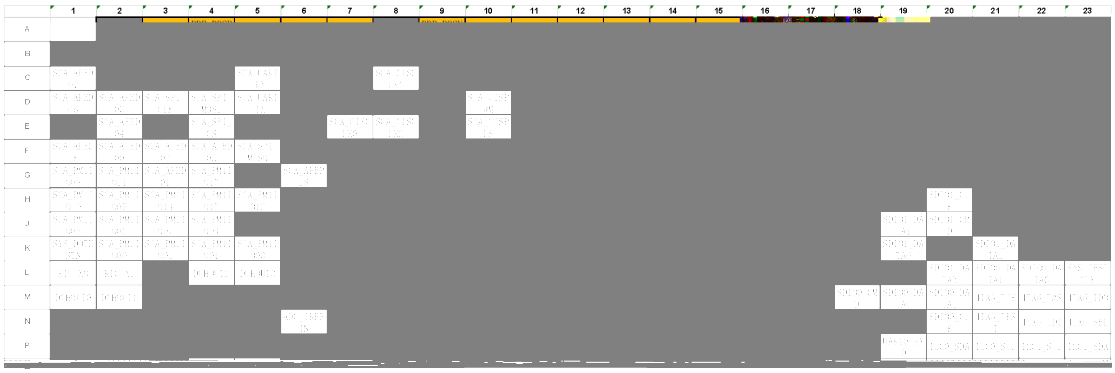
6- 2

Profile Feature		Pb-Free Assembly
Average ramp-up rate (Tsmax to Tp)		3°C/second max.
Preheat	Temperature Min (Tsmin)	150 °C
	Temperature Max (Tsmax)	200 °C
	Time (Tsmin to Tsmax) (ts)	60-180 seconds
Time maintained above	Temperature (TL)	217 °C
	Time (tL)	60-150 seconds
Peak Temperature (Tp)		245°C
Time within 5°C of actual Peak Temperature (tp)2		20-40 seconds
Ramp-down Rate		6 °C/second max.
Time 25°C to Peak Temperature		8 minutes max.

6.1

7

7.1



7.1

7- 1

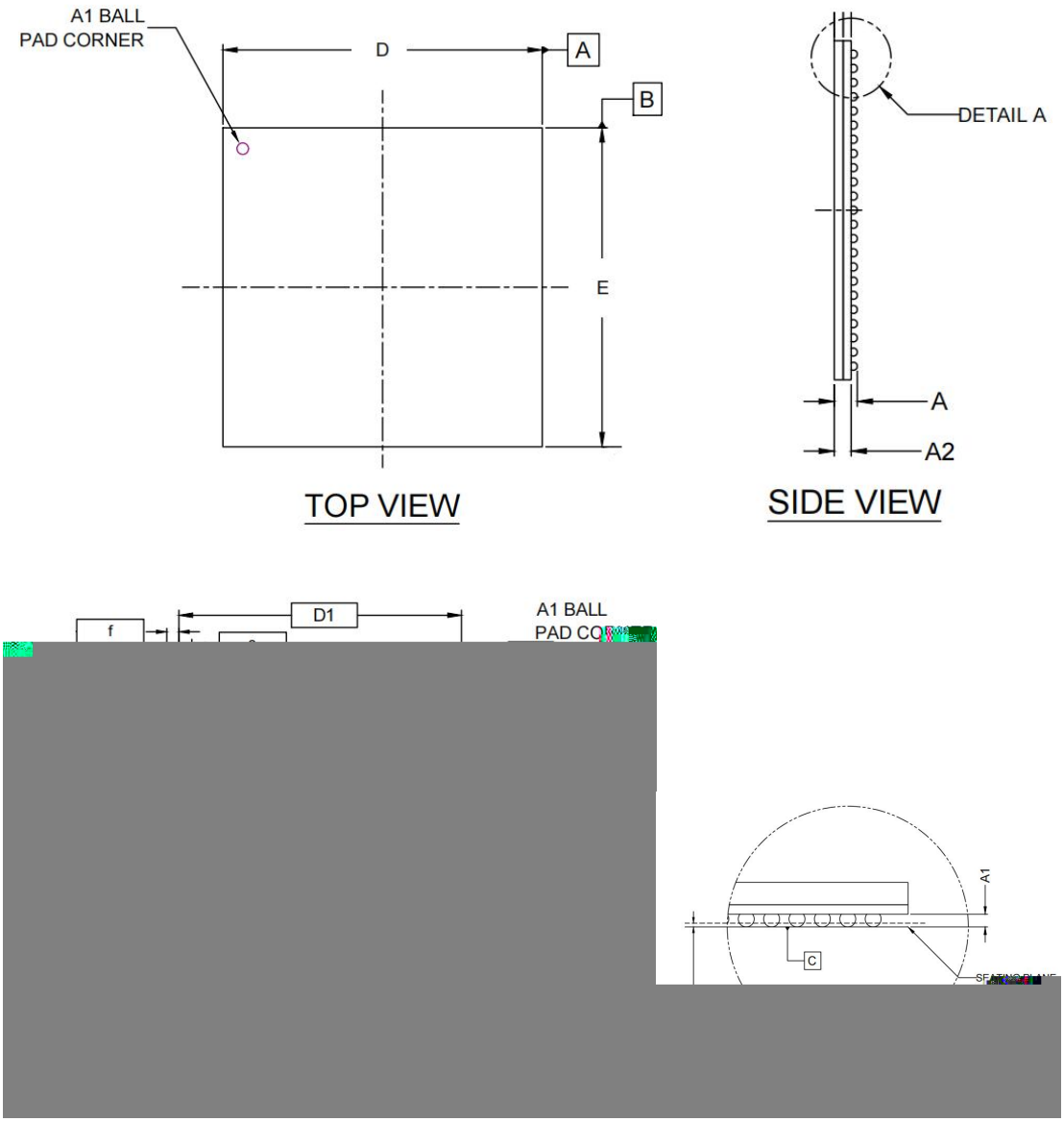
	1	2	3	4	5
A		VSS	DDR_DQ03	DDR_DQSP0	DDR_DQM0
B	VSS	DDR_DQ07	DDR_DQ05	DDR_DQSN0	DDR_DQ02
C	SCA_AFED07	DDR_DQ04	DDR_DQ06	VSS	SCA_UART_RX
D	SCA_AFED06	SCA_AFED03	SCA_SPI_CLK	SCA_SPI_MOSI	SCA_UART_TX
E	VSS	SCA_AFED04	VSS	SCA_SPI_CSN	<DUMMY_NET>
F	SCA_AFECLK	SCA_AFED00	SCA_AFED02	SCA_AFED05	SCA_SPI_MISO
G	SCA_PM1IO08	SCA_PM1IO11	SCA_AFED01	SCA_PM1IO13	VSS
H	SCA_PM1IO10	SCA_PM1IO09	SCA_PM1IO14	SCA_PM1IO15	SCA_PM1IO12
J	SCA_PM1IO06	SCA_PM1IO05	SCA_PM1IO07	SCA_PM1IO04	VSS
K	SYS_DOTESTN	SCA_PM1IO00	SCA_PM1IO02	SCA_PM1IO01	SCA_PM1IO03
L	RTC_XO	RTC_XI	VSS	DCHOUT2	DCHOUT3
M	DCHOUT0	DCHOUT1	<DUMMY_NET>	VSS	<DUMMY_NET>
N	VSS	<DUMMY_NET>	<DUMMY_NET>	<DUMMY_NET>	VSS
P	<DUMMY_NET>	<DUMMY_NET>	<DUMMY_NET>	<DUMMY_NET>	VSS
R	<DUMMY_NET>	<DUMMY_NET>	<DUMMY_NET>	PRT_PM0IO24	PRT_PM0IO18
T	VSS	<DUMMY_NET>	PRT_PM0IO15	PRT_PM0IO21	VSS
U	<DUMMY_NET>	<DUMMY_NET>	PRT_PM0IO31	PRT_PM0IO23	PRT_PM0IO12
V	PRT_PM0IO29	PRT_PM0IO30	PRT_PM0IO25	PRT_PM0IO20	PRT_PM0IO10
W	VSS	PRT_PM0IO28	VSS	PRT_PM0IO19	VSS
Y	PRT_PM0IO26	PRT_PM0IO27	PRT_PM0IO16	PRT_PM0IO09	PRT_PM0IO04
AA	PRT_PM0IO22	PRT_PM0IO17	PRT_PM0IO13	PRT_PM0IO05	PRT_PM0IO07
AB	VSS	PRT_PM0IO14	PRT_PM0IO08	PRT_PM0IO06	PRT_VIDOUT13
AC	VSS	VSS	PRT_PM0IO11	VSS	PRT_VIDOUT12

	6	7	8	9	10
A	DDR_DQ00	DDR_DQ15	VSS	DDR_DQSN1	DDR_DQ11
B	DDR_DQ01	DDR_DQ12	DDR_DQ13	DDR_DQSP1	DDR_DQ10
C	VSS	DDR_DQ14	SCA_CISCLK1	<DUMMY_NET>	DDR_A14
D	VSS	<DUMMY_NET>	VSS	<DUMMY_NET>	SCA_CISPWM
E	VSS	SCA_CISCLK0	SCA_CISCLK2	<DUMMY_NET>	SCA_CISPLS
F	VSS	VSS	VDDIO_DDR	VDDIO_DDR	VDDIO_DDR
G	SCA_AFEPLS	<DUMMY_NET>	<DUMMY_NET>	VSS	<DUMMY_NET>
H	VSS	<DUMMY_NET>	VSS	<DUMMY_NET>	VSS
J	<DUMMY_NET>	<DUMMY_NET>	<DUMMY_NET>	VSS	VDD_CORE
K	VDD_OSC_RTC	VDD_CORE_RTC	VSS	VDD_CORE	VSS
L	VSS_RTC	<DUMMY_NET>	VDD_3V3_DAC	VSS	VDD_CORE
M	<DUMMY_NET>	<DUMMY_NET>	VSS_DAC	VDD_CORE	VSS
N	<DUMMY_NET>	<DUMMY_NET>	VSS	VSS	VDD_CORE
P	<DUMMY_NET>	<DUMMY_NET>	VSS	VDD_CORE	VSS
R	<DUMMY_NET>	VSS	<DUMMY_NET>	VSS	VDD_CORE
T	VSS_LVDS	VDD_3V3_LVDS	VSS	VDD_3V3	VSS
U	<DUMMY_NET>	<DUMMY_NET>	<DUMMY_NET>	<DUMMY_NET>	VSS
V	PRT_PM0IO01	PRT_PM0IO03	<DUMMY_NET>	SYSRESETN	<DUMMY_NET>
W	PRT_PM0IO02	VSS	VSS	PRT_UART_RX	PRT_I2C0_SCL
Y	PRT_PM0IO00	PRT_I2C1_SDA	PRT_I2C1_SCL	PRT_UART_TX	PRT_SPI_MISO
AA	VSS	PLTRSTN	VSS	VSS	PRT_SPI_CSN
AB	PRT_VIDOUT15	PRT_VIDOUT09	PRT_VIDOUT05	PRT_VIDOUT01	PRT_VIDOUT11
AC	PRT_VIDOUT14	PRT_VIDOUT08	PRT_VIDOUT04	PRT_VIDOUT00	PRT_VIDOUT10

	11	12	13	14	15
A	DDR_DQ09	DDR_DQM1	DDR_BA2	DDR_A06	DDR_A08
B	DDR_DQ08	DDR_RESETN	DDR_A09	VSS	DDR_A02
C	VSS	DDR_CKE0	DDR_A07	DDR_A05	<DUMMY_NET>
D	DDR_A12	<DUMMY_NET>	DDR_A04	VSS	<DUMMY_NET>
E	DDR_A15	<DUMMY_NET>	DDR_A11	DDR_A01	<DUMMY_NET>
F	VDDIO_DDR	VDDIO_DDR	VDDIO_DDR	VDDIO_DDR	VDDIO_DDR
G	VSS	<DUMMY_NET>	VSS	<DUMMY_NET>	VSS
H	<DUMMY_NET>	VSS	<DUMMY_NET>	VSS	<DUMMY_NET>
J	VSS	VDD_CORE	VSS	VDD_CORE	VSS
K	VDD_CORE	VSS	VDD_CORE	VSS	VDD_CORE
L	VSS	VDD_CORE	VSS	VDD_CORE	VSS
M	VDD_CORE	VSS	VDD_CORE	VSS	VDD_CORE
N	VSS	VDD_CORE	VSS	VDD_CORE	VSS
P	VDD_CORE	VSS	VDD_CORE	VSS	VDD_CORE
R	VSS	VDD_CORE	VSS	VDD_CORE	VSS
T	VDD_3V3	VSS	VDD_3V3	VSS	VDD_3V3
U	VSS	<DUMMY_NET>	VDD_3V3_USB	VDD_3V3_USB	USB_XO1
V	<DUMMY_NET>	VSS	<DUMMY_NET>	VSS	USB_XI1
W	PRT_I2C0_SDA	GMAC0_RX_CLK	GMAC0_TCTL	<DUMMY_NET>	OTG_OC
Y	PRT_SPI_MOSI	GMAC0_RXD1	GMAC0_MDIO	GMAC0_TXD3	VSS
AA	PRT_SPI_CLK	GMAC0_RXD0	GMAC0_RXD2	GMAC0_TXD1	OTG_VBUS
AB	PRT_VIDOUT07	PRT_VIDOUT03	SYSCLK	GMAC0_RXD3	GMAC0_TXD2
AC	PRT_VIDOUT06	PRT_VIDOUT02	GMAC0_RCTL	VSS	GMAC0_TXD0

	20	21	22	23
A	DDR_DQ16	DDR_DQSP2	VSS	VSS
B	DDR_DQM2	DDR_DQSN2	DDR_DQ19	VSS
C	DDR_WEN	DDR_DQ17	DDR_DQ21	DDR_DQ23
D	<DUMMY_NET>	DDR_DQ18	DDR_DQ20	DDR_DQ22
E	<DUMMY_NET>	VSS	DDR_DQ24	VSS
F	<DUMMY_NET>	DDR_DQM3	DDR_DQ25	DDR_DQ26
G	<DUMMY_NET>	VSS	DDR_DQ27	VSS
H	SDIO1_CLK	<DUMMY_NET>	DDR_DQSP3	DDR_DQSN3
J	SDIO1_CMD	<DUMMY_NET>	DDR_DQ29	DDR_DQ31
K	VSS	SDIO1_DATA2	DDR_DQ30	DDR_DQ28
L	SDIO1_DATA3	SDIO0_DATA1	SDIO0_DATA3	SYS_TESTCLK
M	SDIO0_DATA2	JTAG_TCK	JTAG_TMS	JTAG_TDO
N	SDIO0_CLK	JTAG_TRST	JTAG_TDI	JTAG_SEL
P	I2C0_SDA	I2C0_SCL	I2C1_SCL	I2C1_SDA
R	UART1_RXD	SPI1_CSN	SPI1_MISO	SPI1_CLK
T	PM2IO00	PM2IO01	SPI0_MOSI	SPI1_MOSI
U	PM2IO03	PM2IO02	SPI0_CSN	SPI0_MISO
V	PM2IO04	PM2IO15	USB0_OC	SPI0_CLK
W	PM2IO09	PM2IO06	PM2IO11	USB1_OC
Y	GMAC1_TX_CLK_O	PM2IO08	VSS	PM2IO05
AA	VSS_SOC_PLL	PM2IO13	PM2IO10	PM2IO12
AB	USB0_DP	USB1_DP	PM2IO07	VSS
AC	USB0_DM	USB1_DM	VSS	VSS

7.2


A1 BALL
PAD CORNER
D
A
B
E
TOP VIEW
DETAIL A
A
A2
SIDE VIEW
f
D1
A1 BALL
A1
C

7.2

7- 2

NOTE:

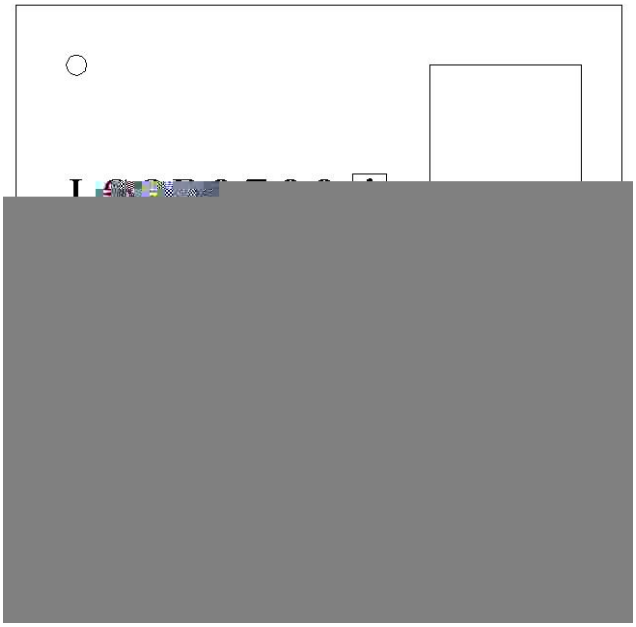
1. DIMENSIONS ARE IN MILLIMETERS.
2. ALL DIMENSIONS AND TOLERANCE CONFORM TO ASME Y14.5M-2009.
3. TERMINAL POSMONS DESIGNATION PER JESD 95.
4. REFLOW BALL DIAMETER.
5. DIMENSION “b” IS MEASURED AT THE MAXIMUM SOLDER BALL DIAMETER PARALLEL TO PRIMARY DATUM C.
6. RAW SOLDER BALL SIZE DURING ASSEMBLY IS

8

8-1

JTAG	JTAG_TRST/TDI 10Kohm
	USB
	10Kohm
NC	

9



9.1

a) ○

b) LS2P0500 LS2P0500 A -i

c) CHN YYWW VV H

d) VDAAAAAAANNNN

e) LOONGSON®

f) c
