2P0500

V1.02

2025 09

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2P0500 / SOC

A4 2P0500

2P0500

- LA364 64 L1 Cache(I/D) 32KB L2 Cache 512KB 750MHz
- LA132 32 400MHz
- 1 32 DDR3
- 2 10M/100M/1000M GMAC RGMII/MII
- 3 USB2.0 HOST 1 OTG
- 4 SPI 1
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-
- 1 4 8 DA
- 4 I2C
- 8 UART
- 2 SDIO
- 40 PWM
- 3 PMIO
- 139 GPIO
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- RTC/HPET
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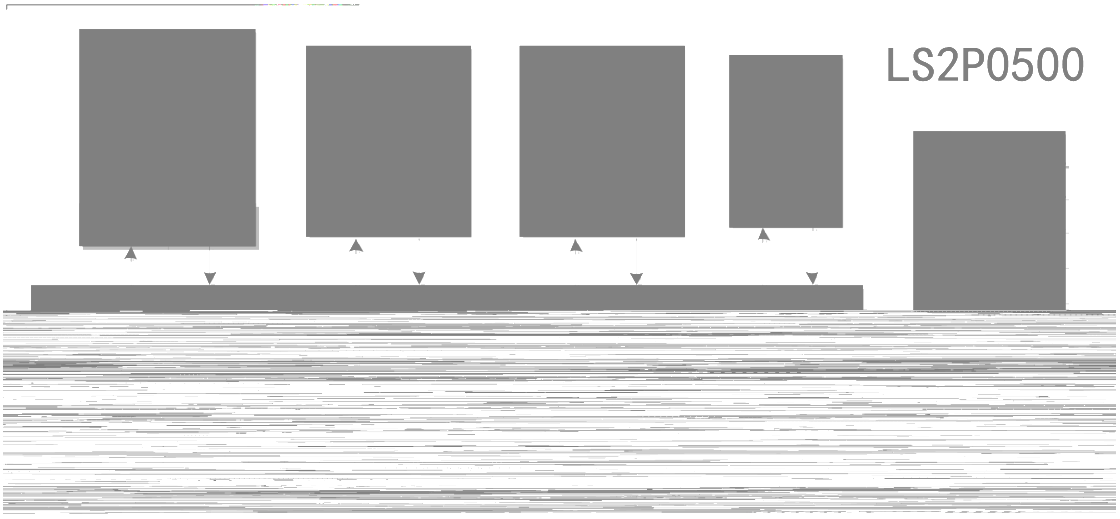
1.1

2P0500

Cache IO Cache Cache IODMA GMAC USB IMAGE PRINT SCAN I2C UART

2P0500 1-1



1- 1 5 i ¢

- OHCI
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1.2.4 GMAC

- 10/100/1000Mbps MAC
- IEEE 802.3
- PHY RGMII/MII
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- Timestamp
- CSMA/CD
- CRC

1.2.5 SPI

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- 4
- (SPI0)
- I/O SPI Flash

1.2.6 UART

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1.2.7 I²C

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1.2.8

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1.2.9

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1.2.10 DA

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1.2.11 PMIO

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1.2.12 PWM

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1.2.13 SDIO

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1.2.14 HPET

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1.2.15 RTC

- 0.1
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1.2.16 GPIO

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1.2.17 Watchdog

- 32
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1.2.18

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1.2.19

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2

2.1

DDR_CKP0 DDR_CKN0	DIFF OUT	DDR3 SDRAM
DDR_ODT0	O	DDR3 SDRAM ODT
DDR_RESETN	O	DDR3 SDRAM

2.3 USB

2- 3 USB

USB[1:0]_XI USB[1:0]_XO	I/O	USB0~1
USB_TXRTUNE[1:0]	A	200ohm/1%
USB[1:0]_DP	I/O	USB D+
USB[1:0]_DM	I/O	USB D-
USB[1:0]_OC	I	USB0~1
OTG_DRVBUS	O	OTG DRVBUS
OTG_DP	I/O	OTG D+
OTG_DM	I/O	OTG D-
OTG_TXRTUNE	A	200ohm/1%
OTG_XI OTG_XO	I/O	OTG
OTG_ID	I	OTG ID
OTG_VBUS	A	OTG VBUS

2.4 GMAC

2- 4 GMAC

GMAC[1:0]_TX_CLK_O	O	RGMII
GMAC[1:0]_TX_CLK_I	I	RGMII ( )
GMAC_TX_CTL	O	RGMII
GMAC_TXD[3:0]	O	RGMII
GMAC[1:0]_RX_CLK_I	I	RGMII
GMAC_RX_CTL	I	RGMII
GMAC_RXD[3:0]	I	RGMII
GMAC_MDCK	O	SMA
GMAC_MDIO	I/O	SMA

2.5 SPI

2- 5 SPI

SPI[1:0]_CLK	O	SPI0~1

SPI[1:0]_CSN	O	SPIO~1
SPI[1:0]_MOSI	O	SPIO~1
SPI[1:0]_MISO	I	SPIO~1
PRT_SPI_CLK	O	SPI
PRT_SPI_CSN	O	SPI
PRT_SPI_MOSI	O	SPI
PRT_SPI_MISO	I	SPI
SCA_SPI_CLK	O	SPI
SCA_SPI_CSN	O	SPI
SCA_SPI_MOSI	O	SPI
SCA_SPI_MISO	I	SPI

2.6 UART

2- 6 UART

UART[1:0]_TXD	O	O~1
UART[1:0]_RXD	I	O~1
PRT_UART_TXD	O	
PRT_UART_RXD	I	
SCA _UART_TXD	O	
SCA _UART_RXD	I	

2.7 I²C

2- 7 I²C

I2C[1:0]_SCL	O	I2CO~1
I2C[1:0]_SDA	I/O	I2CO~1
PRT_I2C[1:0] _SCL	O	I2CO~1
PRT_I2C[1:0] _SDA	I/O	I2CO~1

2.8 P

2- 8 Printer

PRT_VIDOUT[15:0]	O	LVDS TTL

2.9 S

2- 9 Scanner

SCA_AFECLK	O	AFE

SCA_PLS	0	AF

VDDIO_DDR	1.5V	DDR3 1.5V
DDR_VREF	0.75V	DDR3
VDD_3V3	3.3V	IO PAD 3.3V
VDD_3V3_USB	3.3V	USB PHY 3.3V
VDD_RTC	3V	RTC
VDD_3V3_DAC	3.3V	DA 3.3V
VDD_3V3_LVDS	3.3V	LVDS 3.3V
VDD_3V3_THSENS	3.3V	THSENS 3.3V
VSS	0V	
VSS_RTC	0V	RTC
VSS_DAC	0V	DAC
VSS_LVDS	0V	LVDS
VSS_NODE_PLL	0V	NODE PLL
VSS_DDR_PLL	0V	DDR PLL
VSS_SOC_PLL	0V	SOC PLL

2.15

2- 15

DOTESTn	I	(RTC) 0: 1:

2.16 JTAG

2- 16 JTAG

JTAG_SEL	I	JTAG (0 JTAG 1 JTAG)
JTAG_TCK	I	JTAG
JTAG_TDI	I	JTAG
JTAG_TMS	I	JTAG
JTAG_TRST	I	JTAG
JTAG_TDO	O	JTAG

2.17

2- 17

SYSCLK	I	100MHz
SYSRESETN	I	
SYSPLTRSTN	O	
SYS_TESTCLK	I	

RTC_XI RTC_XO	I/O	RTC (32.768KHz)

2.18

2- 18

PMOIO[0]	I	0=SPI 1=SDIO
PMOIO[2:1]	I	PLL 00= 01= 10= 11=bypass
PMOIO[3]	I	SDIO0 0=SDIO 1=EMMC
PMOIO[4]	I	SDIO1 0=SDIO 1=EMMC
PMOIO[6:5]	I	OTG 00= (XI/XO) 01/10= (XO) 11=

2.19 H

main_spi1_miso	pm1io[5]	main_uart0_ri	MAIN_GPIO13
main_spi1_mosi	pm1io[6]	main_uart1_rts	MAIN_GPIO14
main_spi1_cs	pm1io[7]	main_uart1_cts	MAIN_GPIO15
sdio0_clk	pm0io[0]	-	MAIN_GPIO16
sdio0_cmd	pm0io[1]	main_spi0_cs[1]	MAIN_GPIO17
sdio0_d[0]	pm0io[2]	main_spi0_cs[2]	MAIN_GPIO18
sdio0_d[1]	pm0io[3]	main_spi0_cs[3]	MAIN_GPIO19
sdio0_d[2]	pm0io[4]	main_pwm[0]	MAIN_GPIO20
sdio0_d[3]	pm0io[5]	main_pwm[1]	MAIN_GPIO21
sdio1_clk	pm0io[6]	main_pwm[2]	MAIN_GPIO22
sdio1_cmd	pm0io[7]	main_pwm[3]	MAIN_GPIO23
sdio1_d[0]	pm0io[8]	main_pwm[4]	MAIN_GPIO24
sdio1_d[1]	pm0io[9]	main_pwm[5]	MAIN_GPIO25
sdio1_d[2]	pm0io[10]	main_pwm[6]	MAIN_GPIO26
sdio1_d[3]	pm0io[11]	main_pwm[7]	MAIN_GPIO27
pm2io[0]	pm0io[12]	main_pwm[0]	MAIN_GPIO28
pm2io[1]	pm0io[13]	main_pwm[1]	MAIN_GPIO29
pm2io[2]	pm0io[14]	main_pwm[2]	MAIN_GPIO30
pm2io[3]	pm0io[15]	main_pwm[3]	MAIN_GPIO31
pm2io[4]	gmac1_rx_ctl	main_pwm[4]	MAIN_GPIO32
pm2io[5]	gmac1_rx[0]	main_pwm[5]	MAIN_GPIO33
pm2io[6]	gmac1_rx[1]	main_pwm[6]	MAIN_GPIO34
pm2io[7]	gmac1_rx[2]	main_pwm[7]	MAIN_GPIO35
pm2io[8]	gmac1_rx[3]	main_pwm[8]	MAIN_GPIO36
pm2io[9]	gmac1_tx_ctl	main_pwm[9]	MAIN_GPIO37
pm2io[10]	gmac1_tx[0]	main_pwm[10]	MAIN_GPIO38
pm2io[11]	gmac1_tx[1]	main_pwm[11]	MAIN_GPIO39
pm2io[12]	gmac1_tx[2]	main_pwm[12]	MAIN_GPIO40
pm2io[13]	gmac1_tx[3]	main_pwm[13]	MAIN_GPIO41
pm2io[14]	gmac1_mdck	main_pwm[14]	MAIN_GPIO42
pm2io[15]	gmac1_mdio	main_pwm[15]	MAIN_GPIO43

2- 20

prt_uart0_rx	pm0io[0]	prt_pwm[0]	PRT_GPIO00
prt_uart0_tx	pm0io[1]	prt_pwm[1]	PRT_GPIO01
prt_i2c0_scl	pm0io[2]	prt_pwm[2]	PRT_GPIO02
prt_i2c0_sda	pm0io[3]	prt_pwm[3]	PRT_GPIO03
prt_i2c1_scl	prt_uart1_rx	prt_pwm[4]	PRT_GPIO04
prt_i2c1_sda	prt_uart1_tx	prt_pwm[5]	PRT_GPIO05
prt_spi_clk	gmac0_col	prt_pwm[6]	PRT_GPIO06
prt_spi_miso	gmac0_crs	prt_pwm[7]	PRT_GPIO07
prt_spi_mosi	gmac0_ptp_trig	prt_pwm[8]	PRT_GPIO08
prt_spi_cs	gmac0_ptp_pps	prt_pwm[9]	PRT_GPIO09
pm0io[0]	prt_vid_out[16]	prt_pwm[10]	PRT_GPIO10
pm0io[1]	prt_vid_out[17]	prt_pwm[11]	PRT_GPIO11
pm0io[2]	prt_vid_out[18]	prt_pwm[12]	PRT_GPIO12

pm0io[3]	prt_vid_out[19]	prt_pwm[13]	PRT_GPIO13
pm0io[4]	prt_vid_out[20]	prt_pwm[14]	PRT_GPIO14
pm0io[5]	prt_vid_out[21]	prt_pwm[15]	PRT_GPIO15
pm0io[6]	prt_vid_out[22]	prt_pwm[16]	PRT_GPIO16
pm0io[7]	prt_vid_out[23]	prt_pwm[17]	PRT_GPIO17
pm0io[8]	prt_pwm[0]	vid_clk[0]	PRT_GPIO18
pm0io[9]	prt_pwm[1]	vid_clk[1]	PRT_GPIO19
pm0io[10]	prt_pwm[2]	vid_clk[2]	PRT_GPIO20
pm0io[11]	prt_pwm[3]	vid_clk[3]	PRT_GPIO21
pm0io[12]	prt_pwm[4]	prt_vid_en[0]	PRT_GPIO22
pm0io[13]	prt_pwm[5]	prt_vid_en[1]	PRT_GPIO23
pm0io[14]	prt_pwm[6]	prt_vid_en[2]	PRT_GPIO24
pm0io[15]	prt_pwm[7]	prt_vid_en[3]	PRT_GPIO25
pm0io[16]	prt_pwm[8]	prt_ovlin[0]	PRT_GPIO26
pm0io[17]	prt_pwm[9]	prt_ovlin[1]	PRT_GPIO27
pm0io[18]	prt_pwm[10]	prt_ovlin[2]	PRT_GPIO28
pm0io[19]	prt_pwm[11]	prt_ovlin[3]	PRT_GPIO29
pm0io[20]	prt_pwm[12]	prt_ovlin[4]	PRT_GPIO30
pm0io[21]	prt_pwm[13]	prt_ovlin[5]	PRT_GPIO31
pm0io[22]	prt_pwm[14]	prt_ovlin[6]	PRT_GPIO32
pm0io[23]	prt_pwm[15]	prt_ovlin[7]	PRT_GPIO33
pm0io[24]	prt_vid_out[24]	prt_ovlin[8]	PRT_GPIO34
pm0io[25]	prt_vid_out[25]	prt_ovlin[9]	PRT_GPIO35
pm0io[26]	prt_vid_out[26]	prt_ovlin[10]	PRT_GPIO36
pm0io[27]	prt_vid_out[27]	prt_ovlin[11]	PRT_GPIO37
pm0io[28]	prt_vid_out[28]	prt_ovlin[12]	PRT_GPIO38
pm0io[29]	prt_vid_out[29]	prt_ovlin[13]	PRT_GPIO39
pm0io[30]	prt_vid_out[30]	prt_ovlin[14]	PRT_GPIO40
pm0io[31]	prt_vid_out[31]	prt_ovlin[15]	PRT_GPIO41
prt_vid_out[0]	pm0io[8]	pm0io[16]	PRT_GPIO42
prt_vid_out[1]	pm0io[9]	pm0io[17]	PRT_GPIO43
prt_vid_out[2]	pm0io[10]	pm0io[18]	PRT_GPIO44
prt_vid_out[3]	pm0io[11]	pm0io[19]	PRT_GPIO45
prt_vid_out[4]	pm0io[12]	pm0io[20]	PRT_GPIO46
prt_vid_out[5]	pm0io[13]	pm0io[21]	PRT_GPIO47
prt_vid_out[6]	pm0io[14]	pm0io[22]	PRT_GPIO48
prt_vid_out[7]	pm0io[15]	pm0io[23]	PRT_GPIO49
prt_vid_out[8]	prt_pwm[16]	pm0io[24]	PRT_GPIO50
prt_vid_out[9]	prt_pwm[17]	pm0io[25]	PRT_GPIO51
prt_vid_out[10]	prt_pwm[18]	pm0io[26]	PRT_GPIO52
prt_vid_out[11]	prt_pwm[19]	pm0io[27]	PRT_GPIO53
prt_vid_out[12]	prt_pwm[20]	pm0io[28]	PRT_GPIO54
prt_vid_out[13]	prt_pwm[21]	pm0io[29]	PRT_GPIO55
prt_vid_out[14]	prt_pwm[22]	pm0io[30]	PRT_GPIO56
prt_vid_out[15]	prt_pwm[23]	pm0io[31]	PRT_GPIO57

2- 21

sca_uart0_rx	pm1io[16]	-	SCA_GPIO00
sca_uart0_tx	pm1io[17]	-	SCA_GPIO01
sca_spi0_clk	pm1io[18]	-	SCA_GPIO02
sca_spi0_cs	pm1io[19]	sca_uart1_rx	SCA_GPIO03
sca_spi0_miso	pm1io[20]	sca_uart1_tx	SCA_GPIO04
sca_spi0_mosi	pm0io[31]	pm1io[31]	SCA_GPIO05
pm1io[0]	pm0io[0]	sca_afesd[8]	SCA_GPIO06
pm1io[1]	pm0io[1]	sca_afesd[9]	SCA_GPIO07
pm1io[2]	pm0io[2]	sca_afesd[10]	SCA_GPIO08
pm1io[3]	pm0io[3]	sca_afesd[11]	SCA_GPIO09
pm1io[4]	pm0io[4]	sca_afesd[12]	SCA_GPIO10
pm1io[5]	pm0io[5]	sca_afesd[13]	SCA_GPIO11
pm1io[6]	pm0io[6]	sca_afesd[14]	SCA_GPIO12
pm1io[7]	pm0io[7]	sca_afesd[15]	SCA_GPIO13
pm1io[8]	pm0io[8]	sca_afepls[1]	SCA_GPIO14
pm1io[9]	pm0io[9]	sca_afepls[2]	SCA_GPIO15
pm1io[10]	pm0io[10]	sca_cispls[1]	SCA_GPIO16
pm1io[11]	pm0io[11]	sca_cisclk[3]	SCA_GPIO17
pm1io[12]	pm0io[12]	sca_cisclk[4]	SCA_GPIO18
pm1io[13]	pm0io[13]	sca_cisclk[5]	SCA_GPIO19
pm1io[14]	pm0io[14]	sca_cisclk[6]	SCA_GPIO20
pm1io[15]	pm0io[15]	-	SCA_GPIO21
sca_afeclk	pm0io[16]	pm1io[16]	SCA_GPIO22
sca_afepls[0]	pm0io[17]	pm1io[17]	SCA_GPIO23
sca_afesd[0]	pm0io[18]	pm1io[18]	SCA_GPIO24
sca_afesd[1]	pm0io[19]	pm1io[19]	SCA_GPIO25
sca_afesd[2]	pm0io[20]	pm1io[20]	SCA_GPIO26
sca_afesd[3]	pm0io[21]	pm1io[21]	SCA_GPIO27
sca_afesd[4]	pm0io[22]	pm1io[22]	SCA_GPIO28
sca_afesd[5]	pm0io[23]	pm1io[23]	SCA_GPIO29
sca_afesd[6]	pm0io[24]	pm1io[24]	SCA_GPIO30
sca_afesd[7]	pm0io[25]	pm1io[25]	SCA_GPIO31
sca_cisclk[0]	pm0io[26]	pm1io[26]	SCA_GPIO32
sca_cisclk[1]	pm0io[27]	pm1io[27]	SCA_GPIO33
sca_cisclk[2]	pm0io[28]	pm1io[28]	SCA_GPIO34
sca_cispls[0]	pm0io[29]	pm1io[29]	SCA_GPIO35
sca_cispwm	pm0io[30]	pm1io[30]	SCA_GPIO36

(SPI0 SDIO0/eMMC0)

GPIO

3

2P0500 3- 1 100MHz

PLL 3 PLL

PLL 3 3 PLL

SYS PLL SYS

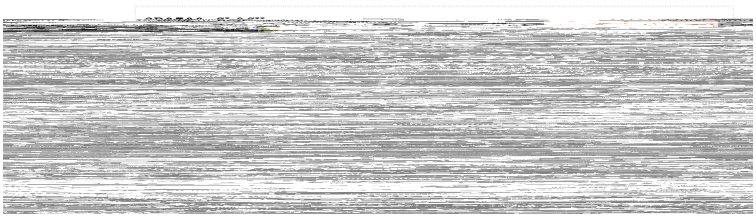
CPU Cache IO

USB GMAC APB

DDR PLL DDR NETWORK IMAGE

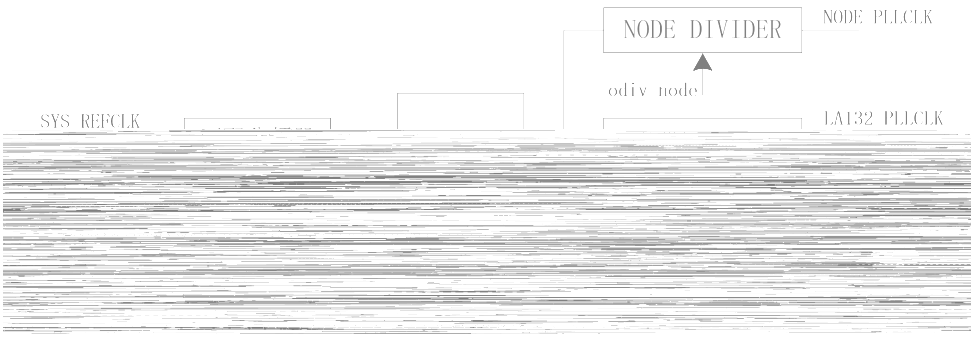
VID PLL Printer Scanner

PLL USB PHY



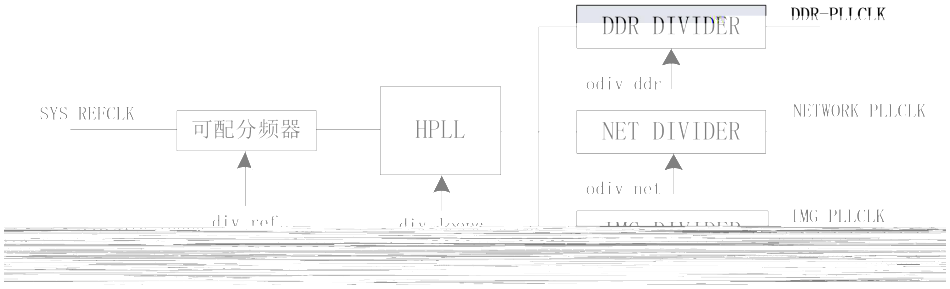
3- 1

3.1 S S PLL



3- 2 SYS PLL

3.2 DDR PLL



3- 3 DDR PLL

3.3 VID PLL

3- 4 SOC PLL

3.4 PLL

3.4.1

3- 2 2P0500

	(MHz)		
SYSCLK	100	I/O	
RTC_XI RTC_XO	32.768K	I/O	RTC
JTAG_TCK	33	I	JTAG
USB_XTAL	25	DIFF IN	USB
DDR_CKp[1:0] DDR_CKn[1:0]	400	DIFF OUT	DDR3 SDRAM
NODE_CLOCK	500~750	-	NODE LA364 SCACHE IODMA L1-XBAR
STABLE_CLOCK	100	-	LA364 STABLE
PR132_CLOCK	100~400	-	132 132
PRXBAR_CLOCK	100~300	-	
PRDEV_CLOCK	100~200	-	APB
SC132_CLOCK	100~400	-	132 132
SCXBAR_CLOCK	100~300	-	
SCDEV_CLOCK	100~200	-	APB
RSMXBAR_CLOCK	100~300	-	RESUME
USB_CLOCK	100~200	-	USB
GMAC_CLOCK	125	-	GMAC
SB_CLOCK	100~200	-	SB (BOOT/CONFBUS)
APB_CLOCK	100~200	-	APB
	100~150	-	AES
SDIOD 9 6 6			

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4.1

- 2P0500 ( )
- OTG
- Dynamic Power Management DPM NODE CORE+SCACHE USB2.0 GMAC
- Dynamic Frequency Scaling DFS DFS LA132
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- 3

4.2

4.1

4.1

	OTG

5

5.1

2P0500

bootcfg

5- 1

PMOIO[0]	I	0=SPI 1=SDIO
PMOIO[2:1]	I	PLL 00= 01= 10= 11=bypass
PMOIO[3]	I	SDIO0 0=SDIO 1=EMMC

0x1400_0000 – 0x1401_ffff	128KB	SYS-CONFBUS	CONFBUS(/ /)
0x1402_0000 – 0x140f_ffff	1MB-128KB	DEVs(AXI-private)	DEVs(USB/GMAC1/IMGP)
0x1410_0000 – 0x141f_ffff	1MB	DEVs(AXI-resume)	LA364-DEVs(/)
0x1420_0000 – 0x142f_ffff	1MB	DEVs(APB)	LA364-DEVs(/ /)
		Reserved	
0x1500_0000 – 0x150f_ffff	1MB	PR-SRAM	PR-SRAM(/ /)
0x1510_0000 – 0x151f_ffff	1MB	PR-DEVs	PR-DEVs(/ /)
0x1520_0000 – 0x152f_ffff	1MB	SC-DEVs	SC-DEVs(/ /)
		Reserved	
0x1c00_0000 – 0x1c0f_ffff	1MB	BOOT	Boot(/ /)
		Reserved	
0x8000_0000 – 0xffff_ffff	2GB	H-DDR	DDR
(AXI-private)[19:0] Base 0x1400_0000	1MB		
0x0_0000	128KB	CONF/INT	CLK/INT/IOMUX...
0x2_0000	64KB	GMAC1	
0x3_0000	64KB	USB1~2	
0x4_0000	64KB	JBIG*4	Jbig*4 16KB
0x5_0000	64KB	JPEG	
(AXI-Resume)[19:0] Base 0x1410_0000	1MB		
0x0_0000	256KB	OTG	(Resume / /)
0x4_0000	64KB	GMAC0	(Resume / /)
(APB)[19:0] Base 0x1420_0000	1MB		
0x0_0000	4KB	UARTx4	(/ /) 1KB
0x0_1000	4KB	I2Cx2	(/ /) 2KB
0x0_2000	4KB	GPIOx64	(/ /)
0x0_3000	4KB	SPIx1	(/ /)
0x0_4000	4KB	HPETx2	(/ /) 2KB
0x0_5000	4KB	WDTx1	(/ /)
0x0_6000	4KB	PM2IOx1	(/ /)
0x0_7000	4KB	PWMx16	(/ /) 256B 16B
0x0_8000	512B	ENC-DMA0	(/ /)
0x0_8200	512B	ENC-DMA1	(/ /)
0x0_8400	1KB-16B	SM2x1	(/ /)
0x0_87f0	16B	RNGx1	(/ /)
0x0_8800	512B	AESx1	(/ /)
0x0_8a00	512B	DESx1	(/ /)
0x0_8c00	512B	SM3x1	(/ /)
0x0_8e00	512B	SM4x1	(/ /)
0x1_0000	32KB	SDIO0+DMA	(/ /)
0x1_8000	32KB	SDIO1+DMA	(/ /)

5- 3

(unmapped)			
		Reserved	
0x1400_0000 – 0x1400_ffff	64KB	CONFBUS(AXI-CONF)	LA364-CONFBUS(/ /)
0x1410_0000 – 0x141f_ffff	1MB	DEVs(AXI-resume)	LA364-Resume-DEVs(/)
0x1420_0000 – 0x142f_ffff	1MB	DEVs(APB)	LA364-APB-DEVs(/ /)
		Reserved	
0x1500_0000 – 0x150f_ffff	1MB	SRAM(128K)	PR-BOOT/DATA(/ /)
0x1510_0000 – 0x151f_ffff	1MB	DEVs(APB)	PR-DEVs(/ /)
0x1520_0000 – 0x152f_ffff	1MB	SC-DEVs	SC-DEVs(/ /)
		Reserved	
0x1c00_0000 – 0x1c0f_ffff	1MB	BOOT	SYS-BOOT(/)
		Reserved	
0x8000_0000 – 0xffff_ffff	2GB	DDR	DDR/CCIO
(AXI)[19:0] Base 0x1500_0000	1MB		
0x0_0000 – 0x1_ffff	128KB	SRAM (128KB)	PR-BOOT/DATA(/ / PR-SRAM)
(APB)[19:0] Base 0x1510_0000	1MB		
0x0_0000	4KB	UARTx2	(/ /) 2KB
0x0_1000	4KB	I2Cx2	(/ /) 2KB
0x0_2000	4KB	GPIOx96	(/ /)
0x0_3000	4KB	CONF	MAILBOX/CLK/INT/CHIP/MUX...(/ /)
0x0_4000	4KB	DPM	(/ /)
0x0_5000	4KB	DAC	(/ /)
0x0_6000	4KB	Reserved	-
0x0_7000	4KB	PWMx24	(/ /) 24*16B 16B
0x0_8000	4KB	PMOIO	(/ /)
0x0_9000	4KB	SPIx1	(/ /)
0x0_a000	4KB	RTC	(/ /)
0x0_b000	4KB	HPET	(/ /)
0x0_c000	16KB	PR-VIDEO	(/ /)

5- 4

(unmapped)			
		Reserved	
0x1400_0000 – 0x1400_ffff	64KB	CONFBUS(AXI-CONF)	LA364-CONFBUS(/ /)
0x1410_0000 – 0x141f_ffff	1MB	DEVs(AXI-resume)	LA364-Resume-DEVs(/)
0x1420_0000 – 0x142f_ffff	1MB	DEVs(APB)	LA364-APB-DEVs(/ /)
		Reserved	
0x1500_0000 – 0x150f_ffff	1MB	SRAM(128K)	PR-BOOT/DATA(/ /)

0x1510_0000 – 0x151f_ffff	1MB	DEVs(APB)	PR-DEVs(/ /)
0x1520_0000 – 0x152f_ffff	1MB	SC-DEVs	SC-DEVs(/ /)
		Reserved	
0x1c00_0000 – 0x1c0f_ffff	1MB	BOOT	SYS-BOOT(/)
		Reserved	
0x8000_0000 – 0xffff_ffff	2GB	DDR	DDR/CCIO
(APB)[19:0]			
Base 0x1520_0000	1MB		
0x0_0000	4KB		

(1) -

Confbus(AXI)

BOOT(AXI)

DEVs(APB)

OTG/GMAC(Resume)

(2)

PRT (PR-SRAM/DEVs)

(3)

SCAN (SC-DEVs)

2P0500 DMA GMAC USB IMG SDIO

5- 5

5- 5 DMA

(mapped)			
0x0000_0000 – 0x7fff_ffff	2G	DDR	CACHE
0x8000_0000 – 0xffff_ffff	2G	CCIO	DDR CCIO
0x0000_0000 – 0x0001_ffff	128KB	SRAM	GMAC0/OTG

5.3

5.3.1

2P0500

PLL

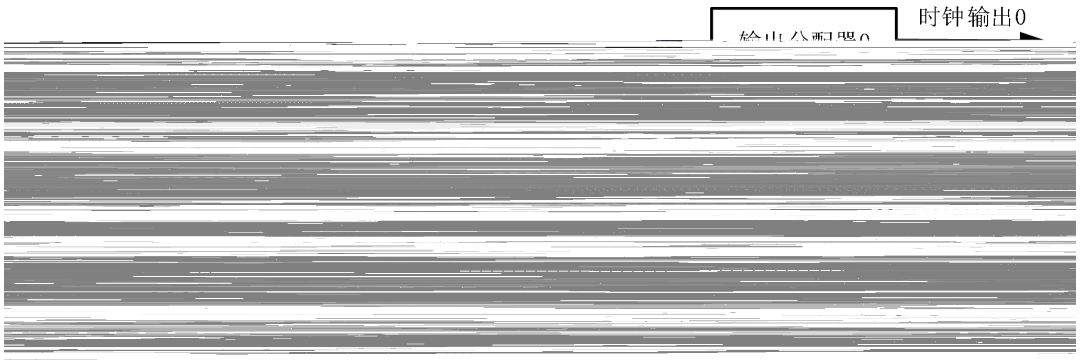
PLL

PLL

5.3.2 PLL

PLL 5- 1 Fin Fref

Fvco PLL



5- 1 PLL

clock_out = refclk / div_ref * loopc / divoutN

2P0500 refclk 100MHz refclk / div_ref
20 ~ 40MHz refclk / div_ref * loopc 1.2GHz ~ 3.2GHz

PLL 5-6

5- 6 PLL

pll_div_out0	7	R/W	PLL 0
pll_div_out1	7	R/W	PLL 1
pll_div_out2	7	R/W	PLL 2

pll_loopc	9	R/W	PLL
pll_div_ref	7	R/W	PLL
pll_locked	1	RO	PLL
sel_pll_out0	1	R/W	PLL 0
sel_pll_out1	1	R/W	PLL 1
sel_pll_out2	1	R/W	PLL 2
set_pll_param	1	R/W	PLL
pll_bypass	1	R/W	PLL bypass
pll_pd	1	R/W	PLL powerdown

5.3.3

2P0500

- USB GMAC
-
-

5.4

2P0500

,

5- 7

0x14000100	MAIN_CHIP_CTRL0	0
0x14000104	MAIN_CHIP_CTRL1	1
0x14000108	MAIN_CHIP_CTRL2	2
0x1400010c	MAIN_CHIP_CTRL3	3
0x14000110	MAIN_CHIP_CTRL4	4
0x14000114	MAIN_CHIP_CTRL5	5
0x14000120	MAIN_CHIP_SAMP0	0
0x14000124	MAIN_CHIP_SAMP1	1
0x14000130	MAIN_CHIP_HPT0	32
0x14000134	MAIN_CHIP_HPT1	32
0x14000490	MAIN_GPIO_CFG0	GPIO00~15
0x14000494	MAIN_GPIO_CFG1	GPIO16~31
0x14000498	MAIN_GPIO_CFG2	GPIO32~47
0x14000500	USB_PHY0	USB PHY 0
0x14000504	USB_PHY1	USB PHY 1

0x14001040	CORE_INTISR0	CORE 32
0x14001044	INTISR0	32
0x14001048	CORE_INTISR1	CORE 32
0x1400104c	INTISR1	32
0x14001148	EXTIOI_ACK	
0x14001400	ENTRY0_0	8 [0--7]
0x14001408	ENTRY8_0	8 [8--15]
0x14001410	ENTRY16_0	8 [16--23]
0x14001418	ENTRY24_0	8 [24--31]
0x14001420	INTISR_0	32
0x14001424	INTIEN_0	32
0x14001428	INTSET_0	32
0x1400142c	INTCLR_0	32
0x14001430	INTPOL_0	32 ( )
0x14001434	INTEDGE_0	32 1 0
0x14001440	ENTRY0_1	8 [32--39]
0x14001448	ENTRY8_1	8 [40--47]
0x14001450	ENTRY16_1	8 [48--55]
0x14001458	ENTRY24_1	8 [56--63]
0x14001460	INTISR_1	32
0x14001464	INTIEN_1	32
0x14001468	INTSET_1	32
0x1400146c	INTCLR_1	32
0x14001470	INTPOL_1	32 ( )
0x14001474	INTEDGE_1	32 1 0
0x140014c0	EXTIOI_MAP	
0x14001500	Thsens_int_ctrl_Hi0	0
0x14001504	Thsens_int_ctrl_Hi1	1
0x14001508	Thsens_int_ctrl_Lo0	0
0x1400150c	Thsens_int_ctrl_Lo1	1
0x14001510	Thsens_int_status/clr	
0x14001514	Thsens_value	
0x14001520	Thsens_scale_hi0	0
0x14001524	Thsens_scale_hi1	1
0x14001600	EXTIOI_IEN0	0
0x14001604	EXTIOI_IEN1	1

0x14001608	EXTIOI_IEN2	2
0x1400160c	EXTIOI_IEN3	3
0x14001640	EXTIOI_POL0	0
0x14001644	EXTIOI_POL1	1
0x14001648	EXTIOI_POL2	2
0x1400164c	EXTIOI_POL3	3
0x14001700	EXTIOI_ISR0	0
0x14001704	EXTIOI_ISR1	1
0x14001708	EXTIOI_ISR2	2
0x1400170c	EXTIOI_ISR3	3
0x14001800	EXTIOI_CORE_ISR0	CORE 0
0x14001804	EXTIOI_CORE_ISR1	CORE 1
0x14001808	EXTIOI_CORE_ISR2	CORE 2
0x1400180c	EXTIOI_CORE_ISR3	CORE 3
0x14003ff0	CHIP_CHIPID0	0
0x14003ff8	CHIP_CHIPID1	1

5- 8

0x15103000	PLL_SYS_0	SYS-PLL 32
0x15103004	PLL_SYS_1	SYS-PLL 32
0x15103008	PLL_DDR_0	PLL 32
0x1510300c	PLL_DDR_1	PLL 32
0x15103010	PLL_VID_0	VID-PLL 32
0x15103014	PLL_VID_1	VID-PLL 32
0x15103020	FREQSCALE0	0
0x15103024	FREQSCALE1	1
0x15103028	FREQSCALE2	2
0x1510302c	PLLCLK_EN	PLL
0x15103030	PRDEV_CLK_CTRL	
0x15103034	PRDEV_RST_CTRL	
0x15103040	PRT_GPIO_CFG0	GPIO00~15
0x15103044	PRT_GPIO_CFG1	GPIO16~31
0x15103048	PRT_GPIO_CFG2	GPIO32~47
0x1510304c	PRT_GPIO_CFG3	GPIO48~63
0x15103060	PRT_CHIPID0	0
0x15103064	PRT_CHIPID1	1
0x15103068	PRT_CHIPID2	2

0x1510306c	PRT_CHIPID3	3
0x15103070	PRT_CHIP_CTRL0	0
0x15103074	PRT_CHIP_CTRL1	1
0x15103078	PRT_CHIP_SAMP	
0x1510307c	PRT_CHIP_HPT	
0x151030e0	PRT_DEVS_BASE	
0x151030f0	PRT_SHARED_CTRL0	0
0x151030f4	PRT_SHARED_CTRL1	1
0x151030f8	PRT_SHARED_CTRL2	2
0x15103100	PRT_BOOT_ENTRY	
0x15103400	PRT_INT_ISR0	0
0x15103404	PRT_INT_IEN0	0
0x1510340c	PRT_INT_CLR0	0
0x15103410	PRT_INT_POL0	0
0x15103414	PRT_INT_EDGE0	0
0x15103418	PRT_INT_DUAL0	0
0x15103420	PRT_INT_ISR1	1
0x15103424	PRT_INT_IEN1	1
0x1510342c	PRT_INT_CLR1	1
0x15103430	PRT_INT_POL1	1
0x15103434	PRT_INT_EDGE1	1
0x15103438	PRT_INT_DUAL1	1
0x15103440	PRT_INT_ISR2	2
0x15103444	PRT_INT_IEN2	2
0x1510344c	PRT_INT_CLR2	2
0x15103450	PRT_INT_POL2	2
0x15103454	PRT_INT_EDGE2	2
0x15103458	PRT_INT_DUAL2	2
0x15103460	PRT_INT_MAP0	0
0x15103464	PRT_INT_MAP1	1
0x15103468	PRT_INT_MAP2	2
0x1510346c	PRT_INT_MAP3	3
0x15103470	PRT_INT_MAP4	4
0x15103474	PRT_INT_MAP5	5
0x15103800	MLB0_IPI_Status	0 Mailbox IPI_Status
0x15103804	MLB0_IPI_Enable	0 Mailbox IPI_Enalbe
0x15103808	MLB0_IPI_Set	0 Mailbox IPI_Set
0x1510380c	MLB0_IPI_Clear	0 Mailbox IPI_Clear
0x15103810	MLB0_message0	0 Mailbox Message0

0x15103814	MLB0_message1	0 Mailbox Message1
0x15103818	MLB0_message2	0 Mailbox Message2
0x1510381c	MLB0_message3	0 Mailbox Message3
0x15103820	MLB0_message4	0 Mailbox Message4
0x15103824	MLB0_message5	0 Mailbox Message5
0x15103828	MLB0_message6	0 Mailbox Message6
0x1510382c	MLB0_message7	0 Mailbox Message7
0x15103830	MLB1_IPI_Status	1 Mailbox IPI_Status
0x15103834	MLB1_IPI_Enable	1 Mailbox IPI_Enalbe
0x15103838	MLB1_IPI_Set	1 Mailbox IPI_Set
0x1510383c	MLB1_IPI_Clear	1 Mailbox IPI_Clear
0x15103840	MLB1_message0	1 Mailbox Message0
0x15103844	MLB1_message1	1 Mailbox Message1
0x15103848	MLB1_message2	1 Mailbox Message2
0x1510384c	MLB1_message3	1 Mailbox Message3
0x15103850	MLB1_message4	1 Mailbox Message4
0x15103854	MLB1_message5	1 Mailbox Message5
0x15103858	MLB1_message6	1 Mailbox Message6
0x1510385c	MLB1_message7	1 Mailbox Message7
0x15103860	MLB2_IPI_Status	2 Mailbox IPI_Status
0x15103864	MLB2_IPI_Enable	2 Mailbox IPI_Enalbe
0x15103868	MLB2_IPI_Set	2 Mailbox IPI_Set
0x1510386c	MLB2_IPI_Clear	2 Mailbox IPI_Clear
0x15103870	MLB2_message0	2 Mailbox Message0
0x15103874	MLB2_message1	2 Mailbox Message1
0x15103878	MLB2_message2	2 Mailbox Message2
0x1510387c	MLB2_message3	2 Mailbox Message3
0x15103880	MLB2_message4	2 Mailbox Message4
0x15103884	MLB2_message5	2 Mailbox Message5
0x15103888	MLB2_message6	2 Mailbox Message6
0x1510388c	MLB2_message7	2 Mailbox Message7
0x15103890	PRT_MailBox_MAP	MailBox

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0x15202030	SCDEV_CLK_CTRL	
0x15202034	SCDEV_RST_CTRL	
0x15202040	SCA_GPIO_CFG0	GPIO00~15
0x15202044	SCA_GPIO_CFG1	GPIO16~31

0x15202048	SCA_GPIO_CFG2	GPIO32~47
0x15202060	SCA_CHIPID	
0x15202070	SCA_CHIP_CTRL	
0x15202078	SCA_CHIP_SAMP	
0x1520207c	SCA_CHIP_HPT	
0x15202100	SCA_BOOT_ENTRY	
0x15202400	SCA_INT_ISR0	0
0x15202404	SCA_INT_IEN0	0
0x1520240c	SCA_INT_CLR0	0
0x15202410	SCA_INT_POL0	0
0x15202414	SCA_INT_EDGE0	0
0x15202418	SCA_INT_DUAL0	0
0x15202420	SCA_INT_ISR1	1
0x15202424	SCA_INT_IEN1	1
0x1520242c	SCA_INT_CLR1	1
0x15202430	SCA_INT_POL1	1
0x15202434	SCA_INT_EDGE1	1
0x15202438	SCA_INT_DUAL1	1
0x15202440	SCA_INT_ISR2	2
0x15202444	SCA_INT_IEN2	2
0x1520244c	SCA_INT_CLR2	2
0x15202450	SCA_INT_POL2	2
0x15202454	SCA_INT_EDGE2	2
0x15202458	SCA_INT_DUAL2	2
0x15202460	SCA_INT_MAP0	0
0x15202464	SCA_INT_MAP1	1
0x15202468	SCA_INT_MAP2	2
0x1520246c	SCA_INT_MAP3	3
0x15202470	SCA_INT_MAP4	4
0x15202474	SCA_INT_MAP5	5
0x15202800	MLB0_IPI_Status	0 Mailbox IPI_Status
0x15202804	MLB0_IPI_Enable	0 Mailbox IPI_Enalbe
0x15202808	MLB0_IPI_Set	0 Mailbox IPI_Set
0x1520280c	MLB0_IPI_Clear	0 Mailbox IPI_Clear
0x15202810	MLB0_message0	0 Mailbox Message0
0x15202814	MLB0_message1	0 Mailbox Message1
0x15202818	MLB0_message2	0 Mailbox Message2
0x1520281c	MLB0_message3	0 Mailbox Message3
0x15202820	MLB0_message4	0 Mailbox Message4

0x15202824	MLB0_message5	0 Mailbox Message5
0x15202828	MLB0_message6	0 Mailbox Message6
0x1520282c	MLB0_message7	0 Mailbox Message7
0x15202830	MLB1_IPI_Status	1 Mailbox IPI_Status
0x15202834	MLB1_IPI_Enable	1 Mailbox IPI_Enalbe
0x15202838	MLB1_IPI_Set	1 Mailbox IPI_Set
0x1520283c	MLB1_IPI_Clear	1 Mailbox IPI_Clear
0x15202840	MLB1_message0	1 Mailbox Message0
0x15202844	MLB1_message1	1 Mailbox Message1
0x15202848	MLB1_message2	1 Mailbox Message2
0x1520284c	MLB1_message3	1 Mailbox Message3
0x15202850	MLB1_message4	1 Mailbox Message4
0x15202854	MLB1_message5	1 Mailbox Message5
0x15202858	MLB1_message6	1 Mailbox Message6
0x1520285c	MLB1_message7	1 Mailbox Message7
0x15202860	MLB2_IPI_Status	2 Mailbox IPI_Status
0x15202864	MLB2_IPI_Enable	2 Mailbox IPI_Enalbe
0x15202868	MLB2_IPI_Set	2 Mailbox IPI_Set
0x1520286c	MLB2_IPI_Clear	2 Mailbox IPI_Clear
0x15202870	MLB2_message0	2 Mailbox Message0
0x15202874	MLB2_message1	2 Mailbox Message1
0x15202878	MLB2_message2	2 Mailbox Message2
0x1520287c	MLB2_message3	2 Mailbox Message3
0x15202880	MLB2_message4	2 Mailbox Message4
0x15202884	MLB2_message5	2 Mailbox Message5
0x15202888	MLB2_message6	2 Mailbox Message6
0x1520288c	MLB2_message7	2 Mailbox Message7
0x15202890	SCA_MailBox_MAP	Mailbox

5.4.1 0

0 UART GMAC USB

0x14000100

5- 10 0

31:28	uart0_enable	RW	0x0	UART0 UART (uart) Bit0 uart0 Bit1 1 uart1 (bit2 0 uart1 4 bit2 1 2) 0 uart0 8 uart1 Bit2 1 uart2 2 0 uart0 8 uart2 Bit3 1 uart3 2 0 uart0 8 uart3
27:26	hpet_int_ctrl	RW	0x0	hpet0~1 0 (3 1) 1 (3 3)
25:24	Reserved	RO	0x0	-
23:20	conf_usb_flush_idle	RW	0xf	write buffer
19	conf_usb_prefetch	RW	0x0	USB
18	conf_usb_flush_wr	RW	0x0	USB read buffer
17	conf_usb_stop_waw	RW	0x0	USB
16	conf_usb_stop_raw	RW	0x1	USB
15	extioi_en	RW	0x0	1 (/) 0 ( )
14	gmac1_mii_sel	RW	0x0	GMAC1 MII 1 MII 0 RGMII
13:12	usbclk_mode	RW	0x3	2 usb 00 USB0 (12MHz) USB1 USB0 01 USB0~1 XO (12MHz) 10 USB0 XO (12MHz) USB1 USB0 11 USB0 PLL (50MHz) USB1 USB0
11:4	conf_iodma_spare_rd	RW	0x0	iodma
3:2	Reserved	RO	0x0	-
1	ddr3_regs_default	RW	0x0	0 1 CPU
0	ddr3_regs_disable	RW	0x0	DDR DDR (1MB @0x0ff0,0000)

5.4.2 1

1 USB GMAC Cache

0x14000104

5- 11 1

31:28	Reserved	RO	0x0	-
27	scdev_coherent	RW	0x0	DMA CACHE (IO CACHE) 1 CACHE 0 CACHE

26	prdev_coherent	RW	0x0	DMA CACHE (IO CACHE) 1 CACHE 0 CACHE
25	apb_coherent	RW	0x0	APB DMA CACHE (IO CACHE) 1 CACHE 0 CACHE
24	image_coherent	RW	0x0	IMAGE (JBIG+JPEG) CACHE (IO CACHE) 1 CACHE 0 CACHE
23	rsm_coherent	RW	0x0	RESUME (GMAC0+OTG) CACHE (IO CACHE) 1 CACHE 0 CACHE
22	gmac1_coherent	RW	0x0	GMAC1 CACHE (IO CACHE) 1 CACHE 0 CACHE
21	usb_coherent	RW	0x0	USB0~1 CACHE (IO CACHE) 1 CACHE 0 CACHE
20	Reserved	RO	0x0	-
19	scdev_coherent_enable	RW	0x0	DMA CACHE 1 CACHE coherent CACHE 0 CACHE coherent (32) CACHE (1: 0:)
18	prdev_coherent_enable	RW	0x0	DMA CACHE 1 CACHE coherent CACHE 0 CACHE coherent (32) CACHE (1: 0:)
17	apb_coherent_enable	RW	0x0	APB DMA CACHE 1 CACHE coherent CACHE 0 CACHE coherent (32) CACHE (1: 0:)
16	image_coherent_enable	RW	0x0	IMAGE (JBIG+JPEG) CACHE 1 CACHE coherent CACHE 0 CACHE coherent (32) CACHE (1: 0:)
15	rsm_coherent_enable	RW	0x0	RESUME (GMAC0+OTG) CACHE 1 CACHE coherent CACHE 0 CACHE coherent (32) CACHE (1: 0:)
14	gmac1_coherent_enable	RW	0x0	GMAC1 CACHE 1 CACHE coherent CACHE 0 CACHE coherent (32) CACHE (1: 0:)

13	usb_coherent_enable	RW	0x0	USB0~1 CACHE 1 CACHE coherent CACHE 0 CACHE coherent

17:16	aes_wdma_map	RW	0x0	AES DMA 00 DMA 0 01 DMA 1
15	scdev_read_upgrade	RW	0x0	DMA
14	prdev_read_upgrade	RW	0x0	DMA
13	apb_read_upgrade	RW	0x0	APB DMA
12	image_read_upgrade	RW	0x0	IMAGE(JBIG+JPEG)
11	rsm_read_upgrade	RW	0x0	RESUME(GMAC0+OTG)
10	gmac1_read_upgrade	RW	0x0	GMAC1
9	usb_read_upgrade	RW	0x0	USB0~1
8	Reserved	RO	0x0	-
7	scdev_write_upgrade	RW	0x0	DMA
6	prdev_write_upgrade	RW	0x0	DMA
5	apb_write_upgrade	RW	0x0	APB DMA
4	image_write_upgrade	RW	0x0	IMAGE(JBIG+JPEG)
3	rsm_write_upgrade	RW	0x0	RESUME(GMAC0+OTG)
2	gmac1_write_upgrade	RW	0x0	GMAC1
1	usb_write_upgrade	RW	0x0	USB0~1
0	Reserved	RO	0x0	-

5.4.4 3

2 3

0x1400010c

5- 13 3

31:24	Reserved	RO	0x1	-
23	jpeg_clk_ctrl	RW	0x1	JPEG 1 0
22	jbig_clk_ctrl	RW	0x1	JBIG 1 0
21	usb_clk_ctrl	RW	0x1	USB0~1 1 0
20	gmac1_clk_ctrl	RW	0x1	GMAC1 1 0
19	Reserved	RO	0x1	-
18	Reserved	RO	0x1	-
17	apbdev_clk_ctrl	RW	0x1	APB 1 0
16	sdio_clk_ctrl	RW	0x1	SDIO 1 0

15	Reserved	RO	0x1	-
14	sm4_clk_ctrl	RW	0x1	SM4 1 0
13	sm3_clk_ctrl	RW	0x1	SM3 1 0
12	des_clk_ctrl	RW	0x1	DES 1 0
11	aes_clk_ctrl	RW	0x1	AES 1 0
10	rng_clk_ctrl	RW	0x1	RNG 1 0
9	sm2_clk_ctrl	RW	0x1	SM2 1 0
8	encdma_clk_ctrl	RW	0x1	ENCRYPT-DMA 1 0
7	pwm_clk_ctrl	RW	0x1	PWM 1 0
6	pm2io_clk_ctrl	RW	0x1	PM2IO 1 0
5	wdt_clk_ctrl	RW	0x1	WDT 1 0
4	hpet_clk_ctrl	RW	0x1	HPET 1 0
3	spi_clk_ctrl	RW	0x1	SPI 1 0
2	gpio_clk_ctrl	RW	0x1	GPIO 1 0
1	i2c_clk_ctrl	RW	0x1	I2C 1 0
0	uart_clk_ctrl	RW	0x1	UART 1 0

5.4.5 4

4

0x14000110

5- 14 4

31:24	Reserved	RO	0x0	-
23	jpeg_rst_ctrl	RW	0x1	JPEG 1 0
22	jbig_rst_ctrl	RW	0x1	JBIG 1 0
21	usb_rst_ctrl	RW	0x1	USB0~1 1 0
20	gmac1_rst_ctrl	RW	0x1	GMAC1 1 0
19	Reserved	RO	0x1	-
18	Reserved	RO	0x1	-
17	apbdev_rst_ctrl	RW	0x1	APB 1 0
16	sdio_rst_ctrl	RW	0x1	SDIO 1 0
15	Reserved	RO	0x1	-

14	sm4_rst_ctrl	RW	0x1	SM4 1 0
13	sm3_rst_ctrl	RW	0x1	SM3 1 0
12	des_rst_ctrl	RW	0x1	DES 1 0
11	aes_rst_ctrl	RW	0x1	AES 1 0
10	rng_rst_ctrl	RW	0x1	RNG 1 0
9	sm2_rst_ctrl	RW	0x1	SM2 1 0
8	encdma_rst_ctrl	RW	0x1	ENCRYPT-DMA 1 0
7	pwm_rst_ctrl	RW	0x1	PWM 1 0
6	pm2io_rst_ctrl	RW	0x1	PM2IO 1 0
5	wdt_rst_ctrl	RW	0x1	WDT 1 0
4	hpet_rst_ctrl	RW	0x1	HPET 1 0
3	spi_rst_ctrl	RW	0x1	SPI 1 0
2	gpio_rst_ctrl	RW	0x1	GPIO 1 0
1	i2c_rst_ctrl	RW	0x1	I2C 1 0
0	uart_rst_ctrl	RW	0x1	UART 1 0

5.4.6 5

5

0x14000114

5- 15 5

31:0	Reserved	RO	0x0	

5.4.7

0x14000120

5- 16

31:7	Reserved	RO	0x0	-
6:5	otg_clkmode	RO	0x0	OTG 00= (XI/XO) 01/10= (XO) 11=
4	sdio1_mode	RO	0x0	SDIO1 0=SDIO 1=EMMC

3	sdio0_mode	RO	0x0	SDIO0 0=SDIO 1=EMMC
2:1	clk_sel	RO	0x0	PLL 00 PLL (NODE:500M DDR:480M NET:320M) 01 PLL (NODE:725M DDR:600M NET:400M) 10 PLL 11 bypass PLL
0	boot_sel	RO	0x0	0 SPI0 1 SDIO0/eMMC0

5.4.8 0

0 64 0~31

0x14000130

5- 17 0

31:0	CHIP_HPT[31:0]	RW	0x0	64 32

5.4.9 1

1 64 32~63

0x14000134

5- 18 1

31:0	CHIP_HPT[63:32]	RW	0x0	64 32

5.4.10 GPIO0~15

GPIO0~15

0x14000490

5- 19 GPIO0~15

31:30	GPIO15_MUX	RW	0x0	GPIO15 00 GPIO15 01 10 11
29:28	GPIO14_MUX	RW	0x0	GPIO14 00 GPIO14 01 10 11
27:26	GPIO13_MUX	RW	0x0	GPIO13 00 GPIO13 01 10 11
25:24	GPIO12_MUX	RW	0x0	GPIO12 00 GPIO12 01 10 11
23:22	GPIO11_MUX	RW	0x0	GPIO11 00 GPIO11 01 10 11

21:20	GPIO10_MUX	RW	0x0	GPIO10 00 GPIO10 01 10 11
19:18	GPIO09_MUX	RW	0x0	GPIO09 00 GPIO09 01 10 11
17:16	GPIO08_MUX	RW	0x0	GPIO08 00 GPIO08 01 10 11
15:14	GPIO07_MUX	RW	0x0	GPIO07 00 GPIO07 01 10 11
13:12	GPIO06_MUX	RW	0x0	GPIO06 00 GPIO06 01 10 11
11:10	GPIO05_MUX	RW	0x0	GPIO05 00 GPIO05 01 10 11
9:8	GPIO04_MUX	RW	0x0	GPIO04 00 GPIO04 01 10 11
7:6	GPIO03_MUX	RW	0x0	GPIO03 00 GPIO03 01 10 11
5:4	GPIO02_MUX	RW	0x0	GPIO02 00 GPIO02 01 10 11
3:2	GPIO01_MUX	RW	0x0	GPIO01 00 GPIO01 01 10 11
1:0	GPIO00_MUX	RW	0x0	GPIO00 00 GPIO00 01 10 11

5.4.11 GPIO16~31

GPIO16~31

0x14000494

5- 20 GPIO16~31

31:30	GPIO31_MUX	RW	0x0	GPIO31 00 GPIO31 01 10 11
29:28	GPIO30_MUX	RW	0x0	GPIO30 00 GPIO30 01 10 11
27:26	GPIO29_MUX	RW	0x0	GPIO29 00 GPIO29 01 10 11
25:24	GPIO28_MUX	RW	0x0	GPIO28 00 GPIO28 01 10 11
23:22	GPIO27_MUX	RW	0x0	GPIO27 00 GPIO27 01 10 11

21:20	GPIO26_MUX	RW	0x0	GPIO26 00 GPIO26 01 10 11
19:18	GPIO25_MUX	RW	0x0	GPIO25 00 GPIO25 01 10 11
17:16	GPIO24_MUX	RW	0x0	GPIO24 00 GPIO24 01 10 11
15:14	GPIO23_MUX	RW	0x0	GPIO23 00 GPIO23 01 10 11
13:12	GPIO22_MUX	RW	0x0	GPIO22 00 GPIO22 01 10 11
11:10	GPIO21_MUX	RW	0x0	GPIO21 00 GPIO21 01 10 11
9:8	GPIO20_MUX	RW	0x0	GPIO20 00 GPIO20 01 10 11
7:6	GPIO19_MUX	RW	0x0	GPIO19 00 GPIO19 01 10 11
5:4	GPIO18_MUX	RW	0x0	GPIO18 00 GPIO18 01 10 11
3:2	GPIO17_MUX	RW	0x0	GPIO17 00 GPIO17 01 10 11
1:0	GPIO16_MUX	RW	0x0	GPIO16 00 GPIO16 01 10 11

5.4.12 GPIO32~43

GPIO32~43

0x14000498

5- 21 GPIO32~43

31:24	Reserved	RO	0x0	-
23:22	GPIO43_MUX	RW	0x0	GPIO43 00 GPIO43 01 10 11
21:20	GPIO42_MUX	RW	0x0	GPIO42 00 GPIO42 01 10 11
19:18	GPIO41_MUX	RW	0x0	GPIO41 00 GPIO41 01 10 11
17:16	GPIO40_MUX	RW	0x0	GPIO40 00 GPIO40 01 10 11

15:14	GPIO39_MUX	RW	0x0	GPIO39 00 GPIO39 01 10 11
13:12	GPIO38_MUX	RW	0x0	GPIO38 00 GPIO38 01 10 11
11:10	GPIO37_MUX	RW	0x0	GPIO37 00 GPIO37 01 10 11
9:8	GPIO36_MUX	RW	0x0	GPIO36 00 GPIO36 01 10 11
7:6	GPIO35_MUX	RW	0x0	GPIO35 00 GPIO35 01 10 11
5:4	GPIO34_MUX	RW	0x0	GPIO34 00 GPIO34 01 10 11
3:2	GPIO33_MUX	RW	0x0	GPIO33 00 GPIO33 01 10 11
1:0	GPIO32_MUX	RW	0x0	GPIO32 00 GPIO32 01 10 11

5.4.13 USB PHY 0

USB PHY 0 USB 0

0x14000500

5- 22 USB PHY 0

31	Reserved	R/O	0	
30	cfg_fs_data_mod	R/W	0	0: 1:
29	commononn0	R/W	0	1 suspend XO Bias PLL Bias PLL 0 suspend XO Bias PLL
28	dmpulldown0	R/W	0	dm 1 D- 0 D-
27	dppulldown0	R/W	0	dp 1 D+ 0 D+

26:25	txrestune0	R/W	0	11 -4Ω 10 -2Ω 01 00 +1.5Ω
24	txpreemppulsetune0	R/W	0	dp,dm 1 1X 0 2X
23:22	txpreempamptune0	R/W	0	J K K J 11 HS 3X 10 HS 2X 01 HS 1X 00 HS
21:20	txhsxvtune0	R/W	0	dp dm 11 default 10 +15mv 01 -15mv 00 reserved
19:18	txrisetune0	R/W	0	11 -10% 10 default 01 +15% 00 +20%
17:14	txvreftune0	R/W	0	1111 +8.75% 1110 +7.5% 1101 +6.25% 1100 +5% 1011 +3.75% 1010 +2.5% 1001 +1.25% 1000 default 0111 -1.25% 0110 -2.5% 0101 -3.75% 0100 -5% 0011 -6.25% 0010 -7.5% 0001 -8.75% 0000 -10%
13:10	txfslstune0	R/W	0	1111 -5% 0111 -2.5% 0011 default 0001 +2.5% 0000 +5%

9:7	sqrxtune0	R/W	0	111 -20% 110 -15% 101 -10% 100 -5% 011 default 010 +5% 001 +10% 000 +15%
6:4	compdistune0	R/W	0	111 +4.5% 110 +3% 101 +1.5% 100 default 011 -1.5% 010 -3% 001 -4.5% 000 -6%
3:1	otgtune0	R/W	0	Vbus Valid 111 +9% 110 +6% 101 +3% 100 default 011 -3% 010 -6% 001 -9% 000 -12%
0	cfg_en0	R/W	0	0: 1:

5.4.14 USB PHY 1

USB PHY 1 USB 1

0x14000504

5- 23 USB PHY 1

31:30	Reserved	R/O	0	
29	commononn1	R/W	0	1 suspend XO Bias PLL Bias PLL 0 suspend XO Bias PLL
28	dmpulldown1	R/W	0	dm 0 D- 1 D-
27	dppulldown1	R/W	0	dp 0 D+ 1 D+
26:25	txrestune1	R/W	0	11 -4Ω 10 -2Ω 01 00 +1.5Ω

24	txpreemppulsetune1	R/W	0	dp,dm 1 1X 0 2X
23:22	txpreempamptune1	R/W	0	J K K J 11 HS 3X 10 HS 2X 01 HS 1X 00 HS
21:20	txhsxvtune1	R/W	0	dp dm 11 default 10 +15mv 01 -15mv 00 reserved
19:18	txrisetune1	R/W	0	 11 -10% 10 default 01 +15% 00 +20%
17:14	txvreftune1	R/W	0	 1111 +8.75% 1110 +7.5% 1101 +6.25% 1100 +5% 1011 +3.75% 1010 +2.5% 1001 +1.25% 1000 default 0111 -1.25% 0110 -2.5% 0101 -3.75% 0100 -5% 0011 -6.25% 0010 -7.5% 0001 -8.75% 0000 -10%
13:10	txfslstune1	R/W	0	 1111 -5% 0111 -2.5% 0011 default 0001 +2.5% 0000 +5%
9:7	sqrxtune1	R/W	0	 111 -20% 110 -15% 101 -10% 100 -5% 011 default 010 +5% 001 +10% 000 +15%

6:4	compdistune1	R/W	0	111 +4.5% 110 +3% 101 +1.5% 100 default 011 -1.5% 010 -3% 001 -4.5% 000 -6%
3:1	otgtune1	R/W	0	Vbus Valid 111 +9% 110 +6% 101 +3% 100 default 011 -3% 010 -6% 001 -9% 000 -12%
0	cfg_en1	R/W	0	0: 1:

5.4.15 SYS PLL 0

SYS PLL 0 SYS PLL

0x15103000

5- 24 SYS-PLL 0

31:30	Reserved	RO	0x0	
29:24	odiv_node	RW	0x0	NODE PLL 0~63
23:16	div_loopc	RW	0x0	PLL 0~255
13:8	div_refc	RW	0x0	PLL 0~63
7	pll_locked	RO	0x0	PLL 1
6	Reserved	RO	0x0	-
5	pd_pll	RW	0x0	PLL 1
4	bypass	RW	0x0	PLL bypass 1 bypass
3	pll_soft_set	RW	0x0	PLL 1
2	pll_sel_soc	RW	0x0	SOC PLL 1 PLL
1	pll_sel_la132	RW	0x0	LA132 PLL 1 PLL
0	pll_sel_node	RW	0x0	NODE PLL 1 PLL

5.4.16 SYSPLL 1

SYS PLL 1

0x15103004

5- 25 SYS-PLL 1

31:14	Reserved	RO	0x0	-
13:8	odiv_soc	RW	0x0	SOC PLL 0~63
7:6	Reserved	RO	0x0	-
5:0	odiv_la132	RW	0x0	LA132 PLL 0~63

5.4.17 DDR PLL 0

DDR PLL 0 DDR PLL 0

0x15103008

5- 26 DDR-PLL 0

31:30	Reserved	RO	0x0	-
29:24	odiv_ddr	RW	0x0	DDR PLL 0~63
23:16	div_loopc	RW	0x0	PLL 0~255
13:8	div_refc	RW	0x0	PLL 0~63
7	pll_locked	RO	0x0	PLL 1
6	Reserved	RO	0x0	-
5	pd_pll	RW	0x0	PLL 1
4	bypass	RW	0x0	PLL bypass 1 bypass
3	pll_soft_set	RW	0x0	PLL 1
2	pll_sel_img	RW	0x0	IMAGE PLL 1 PLL
1	pll_sel_network	RW	0x0	NETWORK PLL 1 PLL
0	pll_sel_ddr	RW	0x0	DDR PLL 1 PLL

5.4.18 DDR PLL 1

DDR PLL 1 DDR PLL

0x1510300c

5- 27 DDR-PLL 1

31:14	Reserved	RO	0x0	-
13:8	odiv_img	RW	0x0	IMAGE PLL 0~63
7:6	Reserved	RO	0x0	-
5:0	odiv_network	RW	0x0	NETWORK PLL 0~63

5.4.19 VID PLL 0

VID PLL 0 VID PLL

0x15103010

5- 28 VID

4	bypass	RW	0x0	PLL	bypass	1	bypass	
3	pll_soft_set	RW	0x0		PLL	1		
2	pll_sel_gmacbp	RW	0x0	GMAC		PLL	1	PLL
1	pll_sel_scvid	RW	0x0		VIDEO	PLL	1	
					PLL			
0	pll_sel_pr0							

7:4	usb_freqscale	RW	0x7	usb_freqscale[3]:USB freq_mode usb_freqscale[2:0]:USB 0~7 SYS PLL SOC USB/OTG
3:0	node_freqscale	RW	0x7	node_freqscale[3]:NODE freq_mode node_freqscale[2:0]:NODE 0~7 SYS PLL NODE NODE (LA364/SCache/IODMA)

5.4.22 1

1

(1) freq_mode=0 fout=fin*(freqscale[2:0]+1)/8

(2) freq_mode=1 fout=fin/(freqscale[2:0]+1)

0x15103024

5- 31

31:28	aes_freqscale	RW	0x7	aes_freqscale[3]:AES freq_mode aes_freqscale[2:0]:AES 0~7 SYS PLL SOC AES
27:24	rsmxbar_freqscale	RW	0x7	rsmxbar_freqscale[3]:RSMXBAR freq_mode rsmxbar_freqscale[2:0]:RSMXBAR 0~7 SYS PLL LA132 … ? RESUME (GMAC0/OTG)
23:20	Reserved	RO	0x7	-

0xx

3:0	pr132_freqscale	RW	0x7	pr132_freqscale[3]:PR132 freq_mode pr132_freqscale[2:0]:PR132

22	scdev_clken	RW	0x1	scdev 1 0
21	scxbar_clken	RW	0x1	scxbar 1 0
20	sc132_clken	RW	0x1	sc132 1 0
19:17	Reserved	RO	0x7	-
16	prvid_clken	RW	0x1	prvid 1 0
15	prifc_clken	RW	0x1	prifc 1 0
14	prdev_clken	RW	0x1	prdev 1 0
13	prxbar_clken	RW	0x1	prxbar 1 0
12	pr132_clken	RW	0x1	pr132 1 0
11	aes_clken	RW	0x1	aes 1 0
10	rsmxbar_clken	RW	0x1	rsmxbar 1 0
9	jpeg_clken	RW	0x1	jpeg 1 0
8	jbig_clken	RW	0x1	jbig 1 0
7	sdio_clken	RW	0x1	sdio 1 0
6	apb_clken	RW	0x1	apb 1 0
5	boot_clken	RW	0x1	boot 1 0
4	gmac_clken	RW	0x1	gmac 1 0
3	usb_clken	RW	0x1	usb 1 0
2	network_clken	RW	0x1	network 1 0
1	ddr_clken	RW	0x1	ddr 1 0
0	node_clken	RW	0x1	node 1 0

5.4.25

0x15103030

5- 34

31:18	Reserved	RO	0x3fff	-
17	otg_clk_ctrl	RW	0x1	RESUME OTG 1 0
16	gmac0_clk_ctrl	RW	0x1	RESUME GMAC0 1 0
15:10	Reserved	RO	0x3f	-
9	prt_clk_ctrl	RW	0x1	Printer

				1 0
8	hpet_clk_ctrl	RW	0x1	HPET 1 0
7	spi_clk_ctrl	RW	0x1	SPI 1 0
6	pm0io_clk_ctrl	RW	0x1	PM0IO 1 0
5	pwm_clk_ctrl	RW	0x1	PWM 1 0
4	Reserved	RO	0x1	-
3	dpm_clk_ctrl	RW	0x1	DPM 1 0
2	gpio_clk_ctrl	RW	0x1	GPIO 1 0
1	i2c_clk_ctrl	RW	0x1	I2C 1 0
0	uart_clk_ctrl	RW	0x1	clk_ f2c_clk UART NB_ 1 0

5.4.26

5.4.27 GPIO0~15

GPIO0~15

0x1510

5.4.2 GPIO16~31

GPIO16~31

0x15103044

5- 37 GPIO16~31

31:30	GPIO31_MUX	RW	0x0	GPIO31 00 10	GPIO31 01 11
29:28	GPIO30_MUX	RW	0x0	GPIO30 00 10	GPIO30 01 11
27:26	GPIO29_MUX	RW	0x0	GPIO29 00 10	GPIO29 01 11
25:24	GPIO28_MUX	RW	0x0	GPIO28 00 10	GPIO28 01 11
23:22	GPIO27_MUX	RW	0x0	GPIO27 00 10	GPIO27 01 11
21:20	GPIO26_MUX	RW	0x0	GPIO26 00 10	GPIO26 01 11
19:18	GPIO25_MUX	RW	0x0	GPIO25 00 10	GPIO25 01 11
17:16	GPIO24_MUX	RW	0x0	GPIO24 00 10	GPIO24 01 11
15:14	GPIO23_MUX	RW	0x0	GPIO23 00 10	GPIO23 01 11
13:12	GPIO22_MUX	RW	0x0	GPIO22 00 10	GPIO22 01 11
11:10	GPIO21_MUX	RW	0x0	GPIO21 00 10	GPIO21 01 11
9:8	GPIO20_MUX	RW	0x0	GPIO20 00 10	GPIO20 01 11
7:6	GPIO19_MUX	RW	0x0	GPIO19 00 10	GPIO19 01 11
5:4	GPIO18_MUX	RW	0x0	GPIO18 00 10	GPIO18 01 11
3:2	GPIO17_MUX	RW	0x0	GPIO17 00 10	GPIO17 01 11
1:0	GPIO16_MUX	RW	0x0	GPIO16 00 10	′EGPIO16 01 11

5.4.29 GPIO32~47

GPIO32~47

0x15103048

5- 38 GPIO32~47

31:30	GPIO47_MUX	RW	0x0	GPIO47 00 GPIO47 01 10 11
29:28	GPIO46_MUX	RW	0x0	GPIO46 00 GPIO46 01 10 11
27:26	GPIO45_MUX	RW	0x0	GPIO45 00 GPIO45 01 10 11
25:24	GPIO44_MUX	RW	0x0	GPIO44 00 GPIO44 01 10 11
23:22	GPIO43_MUX	RW	0x0	GPIO43 00 GPIO43 01 10 11
21:20	GPIO42_MUX	RW	0x0	GPIO42 00 GPIO42 01 10 11
19:18	GPIO41_MUX	RW	0x0	GPIO41 00 GPIO41 01 10 11
17:16	GPIO40_MUX	RW	0x0	GPIO40 00 GPIO40 01 10 11
15:14	GPIO39_MUX	RW	0x0	GPIO39 00 GPIO39 01 10 11
13:12	GPIO38_MUX	RW	0x0	GPIO38 00 GPIO38 01 10 11
11:10	GPIO37_MUX	RW	0x0	GPIO37 00 GPIO37 01 10 11
9:8	GPIO36_MUX	RW	0x0	GPIO36 00 GPIO36 01 10 11
7:6	GPIO35_MUX	RW	0x0	GPIO35 00 GPIO35 01 10 11
5:4	GPIO34_MUX	RW	0x0	GPIO34 00 GPIO34 01 10 11
3:2	GPIO33_MUX	RW	0x0	GPIO33 00 GPIO33 01 10 11
1:0	GPIO32_MUX	RW	0x0	GPIO32 00 GPIO32 01 10 11

5.4.30 GPIO48~57

GPIO48~57

0x1510304c

5- 39 GPIO48~57

31:20	Reserved	RO	0x0	-
19:18	GPIO57_MUX	RW	0x0	GPIO57 00 GPIO57 01 10 11
17:16	GPIO56_MUX	RW	0x0	GPIO56 00 GPIO56 01 10 11
15:14	GPIO55_MUX	RW	0x0	GPIO55 00 GPIO55 01 10 11
13:12	GPIO54_MUX	RW	0x0	GPIO54 00 GPIO54 01 10 11
11:10	GPIO53_MUX	RW	0x0	GPIO53 00 GPIO53 01 10 11
9:8	GPIO52_MUX	RW	0x0	GPIO52 00 GPIO52 01 10 11
7:6	GPIO51_MUX	RW	0x0	GPIO51 00 GPIO51 01 10 11
5:4	GPIO50_MUX	RW	0x0	GPIO50 00 GPIO49 01 10 11
3:2	GPIO49_MUX	RW	0x0	GPIO49 00 GPIO48 01 10 11
1:0	GPIO48_MUX	RW	0x0	GPIO48 00 GPIO47 01 10 11

5.4.31 0

0 PMOIO RTC

0x15103070

5- 40 0

31:10	Reserved	RO	0x0	-
9	pmOio_extin_sel	RW	0x0	PMOIO EXTIN[31:0] 1 PM1IO_INTCON[31:0] 0 PM1IO_INTCON[31:24] VIDCLK_OUT[7:0] PRT_OVLIN[15:0]
8	printer_exttimin_sel	RW	0x0	16 TIMING 1 PMOIO[31:16] 0 PMOIO[15:00]
7:6	Reserved	RO	0x0	-
5	pr132_nmi	RW	0x0	NMI

4	hpet_int_ctrl	RW	0x0	hp 0 3 1) 1 3 3)
3:1	Reserved	RO	0x0	-
0	conf_rtc_timer_hspeed	RW	0x0	RTC 1 0

5.4.32 1

1 USB GMAC Cache

0x15103074

5- 41 1

31:16	Reserved	RO	0x0	-
15:8	prvidout_lvds_tm	RW	0x0	8 LVDS 1 bypass 0 normal ( )
7:0	prvidout_lvds_pd	RW	0xff	8 LVDS PD 1 powerdown TTL 0 poweron LVDS

5.4.33

0x15103078

5- 42

31:12	Reserved	RO	0x0	-
11	la364_pwroff_sta	RO	0x0	0=POWERON 1=POWEROFF
10	Æ			

				(NODE:500M DDR:480M NET:320M) 01 PLL (NODE:725M DDR:600M NET:400M) 10 PLL 11 bypass PLL
0	boot_sel	RO	0x0	0 SPI0 1 SDIO0/eMMC0

5.4.34

32

0x1510307c

5- 43

31:0	PRCHIP_HPT	RW	0x0	32

5.4.35 DMA

DMA SRAM DMA

0x151030e0

5- 44 DMA

31:16	prdma_base_addr	RW	0x0	DMA prdma_base_addr[0] 0- SRAM(128KB) 1- SRAM(128KB) SRAM prdma_base_addr[15:1] SRAM DMA [31:17]
15:0	prsram_base_addr	RW	0x1500	SRAM [31:16]

5.4.36 0

0 OTG GMAC JTAG

0x151030f0

5- 45 0

31:13	Reserved	RO	0x0	-
12	la364_ram_cg	RW	0x0	RAM
11:10	jtag_mode_config	RW	0x0	JTAG 00 LA364 JTAG 01 PR132 JTAG 10 SC132 JTAG 11 LA364->PR132->SC132 JTAG
9	gmac_test_lpbk	RW	0x0	GMAC0~1 loopback

				1 loopback 0 loopback
8	gmac0_mii_sel	RW	0x0	GMAC0 MII 1 MII 0 RG

28	dmpulldown0	R/W	0	dm 1 D- 0 D-
27	dppulldown0	R/W	0	dp 1 D+ 0 D+
26:25	txrestune0	R/W	0	 11 -4Ω 10 -2Ω 01 00 +1.5Ω
24	txpreemppulsetune0	R/W	0	dp,dm
23:22	txpreempamptune0	R/W	0	 1 1X 0 2X J K K J 11 HS

9:7	sqrxtune0	R/W	0	111 -20% 110 -15% 101 -10% 100 -5% 011 default 010 +5% 001 +10% 000 +15%
6:4	compdistune0	R/W	0	111 +4.5% 110 +3% 101 +1.5% 100 default 011 -1.5% 010 -3% 001 -4.5% 000 -6%
3:1	otgtune0	R/W	0	Vbus Valid 111 +9% 110 +6% 101 +3% 100 default 011 -3% 010 -6% 001 -9% 000 -12%
0	cfg_en0	R/W	0	0: 1:

5.4.39

0x15103100

5- 48

31:0	pr132_boot_entry	RW	0x1c000000	, bit[0] 1- 0- (0x1c000000)

5.4.40 0 MAILBOX

0 MAILBOX

0x15103800

5- 49 0 MAILBOX

31:0	mlb0_ipi_status	RO	0x0	0 Mailbox 1

5.4.41 0 MAILBOX

0 MAILBOX

0x15103804

5- 50 0 MAILBOX

31:0	mlb0_ipi_enable	RW	0x0	0 Mailbox

5.4.42 0 MAILBOX

0 MAILBOX

0x15103808

5- 51 0 MAILBOX

31:0	mlb0_ipi_set	W	-	0 Mailbox 1

5.4.43 0 MAILBOX

0 MAILBOX

0x1510380c

5- 52 0 MAILBOX

31:0	mlb0_ipi_clear	W	-	0 Mailbox 1 1

5.4.44 0 MAILBOX 0~7

0 MAILBOX 0~7

0x15103810~0x1510382c

5- 53 0 MAILBOX 0~7

31:0	mlb0_message7	RW	0x0	0 Mailbox 7
31:0	mlb0_message6	RW	0x0	0 Mailbox 6
31:0	mlb0_message5	RW	0x0	0 Mailbox 5
31:0	mlb0_message4	RW	0x0	0 Mailbox 4
31:0	mlb0_message3	RW	0x0	0 Mailbox 3
31:0	mlb0_message2	RW	0x0	0 Mailbox 2
31:0	mlb0_message1	RW	0x0	0 Mailbox 1
31:0	mlb0_message0	RW	0x0	0 Mailbox 0

5.4.45 1 MAILBOX

1 MAILBOX

0x15103830

5- 54 1 MAILBOX

31:0	mlb1_ipi_status	RO	0x0	1 Mailbox 1

5.4.46 1 MAILBOX

1 MAILBOX

0x15103834

5- 55 1 MAILBOX

31:0	mlb1_ipi_enable	RW	0x0	1 Mailbox

5.4.47 1 MAILBOX

1 MAILBOX

0x15103838

5- 56 1 MAILBOX

31:0	mlb1_ipi_set	W	-	1 Mailbox 1

5.4.48 1 MAILBOX

1 MAILBOX

0x1510383c

5- 57 1 MAILBOX

31:0	mlb1_ipi_clear	W	-	1 Mailbox 1 1

5.4.49 1 MAILBOX 0~7

1 MAILBOX 0~7

0x15103840~0x1510385c

5- 58 1 MAILBOX 0~7

31:0	mlb1_message7	RW	0x0	1 Mailbox 7
31:0	mlb1_message6	RW	0x0	1 Mailbox 6
31:0	mlb1_message5	RW	0x0	1 Mailbox 5
31:0	mlb1_message4	RW	0x0	1 Mailbox 4
31:0	mlb1_message3	RW	0x0	1 Mailbox 3
31:0	mlb1_message2	RW	0x0	1 Mailbox 2
31:0	mlb1_message1	RW	0x0	1 Mailbox 1
31:0	mlb1_message0	RW	0x0	1 Mailbox 0

5.4.50 2 MAILBOX

2 MAILBOX

0x15103860

5- 59 2 MAILBOX

31:0	mlb2_ipi_status	RO	0x0	2 Mailbox 1

5.4.51 2 MAILBOX

2 MAILBOX

0x15103864

5- 60 2 MAILBOX

31:0	mlb2_ipi_enable	RW	0x0	2 Mailbox

5.4.52 2 MAILBOX

2 MAILBOX

0x15103868

5- 61 2 MAILBOX

31:0	mlb2_ipi_set	W	-	2 Mailbox 1

5.4.53 2 MAILBOX

2 MAILBOX

0x1510386c

5- 62 2 MAILBOX

31:0	mlb2_ipi_clear	W	-	2 Mailbox 1 1

5.4.54 2 MAILBOX 0~7

2 MAILBOX 0~7

0x15103870~0x1510388c

5- 63 0 MAILBOX 0~7

31:0	mlb2_message7	RW	0x0	2 Mailbox 7
31:0	mlb2_message6	RW	0x0	2 Mailbox 6
31:0	mlb2_message5	RW	0x0	2 Mailbox 5
31:0	mlb2_message4	RW	0x0	2 Mailbox 4
31:0	mlb2_message3	RW	0x0	2 Mailbox 3
31:0	mlb2_message2	RW	0x0	2 Mailbox 2
31:0	mlb2_message1	RW	0x0	2 Mailbox 1
31:0	mlb2_message0	RW	0x0	2 Mailbox 0

5.4.55 MAILBOX

MAILBOX 0~2 MAILBOX

0x15103890

5- 64 MAILBOX

31:11	Reserved	RO	0x0	-
10:8	mlb2_ipi_map	RW	0x0	2 Mailbox 001:2 Mailbox 010:2 Mailbox 100:2 Mailbox
7	Reserved	RO	0x0	-
6:4	mlb1_ipi_map	RW	0x0	1 Mailbox 001:1 Mailbox 010:1 Mailbox 100:1 Mailbox
3	Reserved	RO	0x0	-
2:0	mlb0_ipi_map	RW	0x0	0 Mailbox 001:0 Mailbox 010:0 Mailbox 100:0 Mailbox

5.4.56

0x15202030

5- 65

31:9	Reserved	RO	0x7fffff	-
8	sc132_clk_ctrl	RW	0x1	1 0
7:6	Reserved	RO	0x3	-
5	scvid_clk_ctrl	RW	0x1	Scanner 1 0
4	hpet_clk_ctrl	RW	0x1	HPET 1 0
3	pm1io_clk_ctrl	RW	0x1	PM1IO 1 0
2	spi_clk_ctrl	RW	0x1	SPI 1 0
1	gpio_clk_ctrl	RW	0x1	GPIO 1 0
0	uart_clk_ctrl	RW	0x1	UART 1 0

5.4.57

0x15202034

5- 66

31:9	Reserved	RO	0x7fffff	-
8	sc132_rst_ctrl	RW	0x1	1 0
7:6	Reserved	RO	0x3	-
5	scvid_rst_ctrl	RW	0x1	Scanner 1 0
4	hpet_rst_ctrl	RW	0x1	HPET 1 0
3	pm1io_rst_ctrl	RW	0x1	PMOIO 1 0
2	spi_rst_ctrl	RW	0x1	SPI 1 0
1	gpio_rst_ctrl	RW	0x1	GPIO 1 0
0	uart_rst_ctrl	RW	0x1	UART 1 0

5.4.58 GPIO0~15

GPIO0~15

0x15202040

5- 67 GPIO0~15

31:30	GPIO15_MUX	RW	0x0	GPIO15 00 GPIO15 01 10 11
29:28	GPIO14_MUX	RW	0x0	GPIO14 00 GPIO14 01 10 11
27:26	GPIO13_MUX	RW	0x0	GPIO13 00 GPIO13 01 10 11
25:24	GPIO12_MUX	RW	0x0	GPIO12 00 GPIO12 01 10 11
23:22	GPIO11_MUX	RW	0x0	GPIO11 00 GPIO12 01 10 11
21:20	GPIO10_MUX	RW	0x0	GPIO10 00 GPIO10 01 10 11
19:18	GPIO09_MUX	RW	0x0	GPIO09 00 GPIO09 01 10 11
17:16	GPIO08_MUX	RW	0x0	GPIO08 00 GPIO08 01 10 11
15:14	GPIO07_MUX	RW	0x0	GPIO07 00 GPIO07 01 10 11
13:12	GPIO06_MUX	RW	0x0	GPIO06 00 GPIO06 01 10 11
11:10	GPIO05_MUX	RW	0x0	GPIO05 00 GPIO05 01 10 11
9:8	GPIO04_MUX	RW	0x0	GPIO04 00 GPIO04 01 10 11
7:6	GPIO03_MUX	RW	0x0	GPIO03 00 GPIO03 01 10 11
5:4	GPIO02_MUX	RW	0x0	GPIO02 00 GPIO02 01 10 11
3:2	GPIO01_MUX	RW	0x0	GPIO01 00 GPIO01 01 10 11
1:0	GPIO00_MUX	RW	0x0	GPIO00 00 GPIO00 01 10 11

5.4.59 GPIO16~31

GPIO16~31

0x15202044

5- 68 GPIO16~31

31:30	GPIO31_MUX	RW	0x0	GPIO31 00 GPIO31 01 10 11
29:28	GPIO30_MUX	RW	0x0	GPIO30 00 GPIO30 01 10 11
27:26	GPIO29_MUX	RW	0x0	GPIO29 00 GPIO29 01 10 11
25:24	GPIO28_MUX	RW	0x0	GPIO28 00 GPIO28 01 10 11
23:22	GPIO27_MUX	RW	0x0	GPIO27 00 GPIO27 01 10 11
21:20	GPIO26_MUX	RW	0x0	GPIO26 00 GPIO26 01 10 11
19:18	GPIO25_MUX	RW	0x0	GPIO25 00 GPIO25 01 10 11
17:16	GPIO24_MUX	RW	0x0	GPIO24 00 GPIO24 01 10 11
15:14	GPIO23_MUX	RW	0x0	GPIO23 00 GPIO23 01 10 11
13:12	GPIO22_MUX	RW	0x0	GPIO22 00 GPIO22 01 10 11
11:10	GPIO21_MUX	RW	0x0	GPIO21 00 GPIO21 01 10 11
9:8	GPIO20_MUX	RW	0x0	GPIO20 00 GPIO20 01 10 11
7:6	GPIO19_MUX	RW	0x0	GPIO19 00 GPIO19 01 10 11
5:4	GPIO18_MUX	RW	0x0	GPIO18 00 GPIO18 01 10 11
3:2	GPIO17_MUX	RW	0x0	GPIO17 00 GPIO17 01 10 11
1:0	GPIO16_MUX	RW	0x0	GPIO16 00 GPIO16 01 10 11

5.4.60 GPIO32~36

GPIO32~36

0x15202048

5- 69 GPI032

4	sdio1_mode	RO	0x0	SDIO1 0=SDIO 1=EMMC
3	sdio0_mode	RO	0x0	SDIO0 0=SDIO 1=EMMC
2:1	clk_sel	RO	0x0	PLL 00 PLL (NODE:500M DDR:480M NET:320M) 01 PLL (NODE:725M DDR:600M NET:400M) 10 PLL 11 bypass PLL
0	boot_sel	RO	0x0	0 SPI0 1 SDIO0/eMMC0

5.4.63

32

0x1520207c

5- 72

		RW	0x0	32

5.4.64

0x15202100

5- 73

31:0	sc132_boot_entry	RW	0x1c000000	, bit[0] 1- 0- (0x1c000000)

5.4.65 0 MAILBOX

0 MAILBOX

0x15202800

5- 74 0 MAILBOX

31:0	mlb0_ipi_status	RO	0x0	0 Mailbox 1

5.4.66 0 MAILBOX

0 MAILBOX

0x15202804

5- 75 0 MAILBOX

31:0	mlb0_ipi_enable	RW	0x0	0 Mailbox

5.4.67 0 MAILBOX

0 MAILBOX

0x15202808

5- 76 0 MAILBOX

31:0	mlb0_ipi_set	W	-	0 Mailbox 1

5.4.68 0 MAILBOX

0 MAILBOX

0x1520280c

5- 77 0 MAILBOX

31:0	mlb0_ipi_clear	W	-	0 Mailbox 1 1

5.4.69 0 MAILBOX 0~7

0 MAILBOX 0~7

0x15202810~0x1520282c

5- 78 0 MAILBOX 0~7

31:0	mlb0_message7	RW	0x0	0 Mailbox 7
31:0	mlb0_message6	RW	0x0	0 Mailbox 6
31:0	mlb0_message5	RW	0x0	0 Mailbox 5
31:0	mlb0_message4	RW	0x0	0 Mailbox 4
31:0	mlb0_message3	RW	0x0	0 Mailbox 3
31:0	mlb0_message2	RW	0x0	0 Mailbox 2
31:0	mlb0_message1	RW	0x0	0 Mailbox 1
31:0	mlb0_message0	RW	0x0	0 Mailbox 0

5.4.70 1 MAILBOX

1 MAILBOX

0x15202830

5- 79 1 MAILBOX

31:0	mlb1_ipi_status	RO	0x0	1 Mailbox 1

5.4.71 1 MAILBOX

1 MAILBOX

0x15202834

5- 80 1 MAILBOX

31:0	mlb1_ipi_enable	RW	0x0	1 Mailbox

5.4.72 1 MAILBOX

1 MAILBOX

0x15202838

5- 81 1 MAILBOX

31:0	mlb1_ipi_set	W	-	1 Mailbox 1

5.4.73 1 MAILBOX

1 MAILBOX

0x1520283c

5- 82 1 MAILBOX

31:0	mlb1_ipi_clear	W	-	1 Mailbox 1 1

5.4.74 1 MAILBOX 0~7

1 MAILBOX 0~7

0x15202840~0x1520285c

5- 83 1 MAILBOX 0~7

31:0	mlb1_message7	RW	0x0	1 Mailbox 7
31:0	mlb1_message6	RW	0x0	1 Mailbox 6
31:0	mlb1_message5	RW	0x0	1 Mailbox 5
31:0	mlb1_message4	RW	0x0	1 Mailbox 4

31:0	mlb1_message3	RW	0x0	1 Mailbox 3
31:0	mlb1_message2	RW	0x0	1 Mailbox 2
31:0	mlb1_message1	RW	0x0	1 Mailbox 1
31:0	mlb1_message0	RW	0x0	1 Mailbox 0

5.4.75 2 MAILBOX

2 MAILBOX

0x15202860

5- 84 2 MAILBOX

31:0	mlb2_ipi_status	RO	0x0	2 Mailbox 1

5.4.76 2 MAILBOX

2 MAILBOX

0x15202864

5- 85 2 MAILBOX

31:0	mlb2_ipi_enable	RW	0x0	2 Mailbox

5.4.77 2 MAILBOX

2 MAILBOX

0x15202868

5- 86 2 MAILBOX

31:0	mlb2_ipi_set	W	-	2 Mailbox 1

5.4.78 2 MAILBOX

2 MAILBOX

0x1520286c

5- 87 2 MAILBOX

31:0	mlb2_ipi_clear	W	-	2 Mailbox 1 1

5.4.79 2 MAILBOX 0~7

2 MAILBOX 0~7

0x15202870~0x1520288c

5- 88 0 MAILBOX 0~7

31:0	mlb2_message7	RW	0x0	2 Mailbox 7
31:0	mlb2_message6	RW	0x0	2 Mailbox 6
31:0	mlb2_message5	RW	0x0	2 Mailbox 5
31:0	mlb2_message4	RW	0x0	2 Mailbox 4
31:0	mlb2_message3	RW	0x0	2 Mailbox 3
31:0	mlb2_message2	RW	0x0	2 Mailbox 2
31:0	mlb2_message1	RW	0x0	2 Mailbox 1
31:0	mlb2_message0	RW	0x0	2 Mailbox 0

5.4.80 MAILBOX

MAILBOX 0~2 MAILBOX

0x15202890

5- 89 MAILBOX

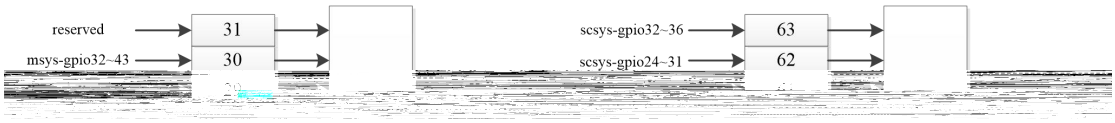
31:11	Reserved	RO	0x0	-
10:8	mlb2_ipi_map	RW	0x0	2 Mailbox 001:2 Mailbox 010:2 Mailbox 100:2 Mailbox
7	Reserved	RO	0x0	-
6:4	mlb1_ipi_map	RW	0x0	1 Mailbox 001:1 Mailbox 010:1 Mailbox 100:1 Mailbox
3	Reserved	RO	0x0	-
2:0	mlb0_ipi_map	RW	0x0	0 Mailbox 001:0 Mailbox 010:0 Mailbox 100:0 Mailbox

5.5

2P0500

5.5.1

64 10


reserved
msys-gpio32~43
31
30
scsys-gpio32~36
scsys-gpio24~31
63
62

5- 2 10

5- 90 IO

0x14001040	CORE_INTISR0	CORE 32
0x14001044	INTISR0	32
0x14001048	CORE_INTISR1	CORE 32
0x1400104c	INTISR1	32
0x14001400	ENTRY0_0	8 [0--7]
0x14001408	ENTRY8_0	8 [8--15]
0x14001410	ENTRY16_0	8 [16--23]
0x14001418	ENTRY24_0	8 [24--31]
0x14001420	INTISR_0	32
0x14001424	INTIEN_0	32
0x14001428	INTSET_0	32
0x1400142c	INTCLR_0	32
0x14001430	INTPOL_0	32 ( )
0x14001434	INTEDGE_0	32 1 0
0x14001440	ENTRY0_1	8 [32--39]
0x14001448	ENTRY8_1	8 [40--47]
0x14001450	ENTRY16_1	8 [48--55]
0x14001458	ENTRY24_1	8 [56--63]
0x14001460	INTISR_1	32
0x14001464	INTIEN_1	32
0x14001468	INTSET_1	32
0x1400146c	INTCLR_1	32
0x14001470	INTPOL_1	32 ( )
0x14001474	INTEDGE_1	32 1 0
0x14001500	Thsens_int_ctrl_Hi0	0
0x14001504	Thsens_int_ctrl_Hi1	1
0x14001508	Thsens_int_ctrl_Lo0	0
0x1400150c	Thsens_int_ctrl_Lo1	1
0x14001510	Thsens_int_status/clr	
0x14001514	Thsens_value	
0x14001520	Thsens_scale_hi0	0
0x14001524	Thsens_scale_hi1	1

2P0500 IO IO

2P0500 IO IO

IO 128 IO IO

IO

IO 64 IO

5- 3 IO

2P0500 IO “ 0 ”

IO 0x14000100

15	extioi_enable	RW	0x0	1 (/) 0 ( )

IO

5-96

EXTINT_IEN EXTINT_ISR EXTINT_ICLR

EXTINT_IEN 1 EXTINT_ISR

1 IO (

) EXTINT_ICLR 1

CORE_EXTISR CORE_EXTICLR

CORE_EXTISR IO IO

IO CORE_EXTICLR

1

IO EXTINT_MAP IO

IO CP0_Status

IP0 IP3

5- 91 IO

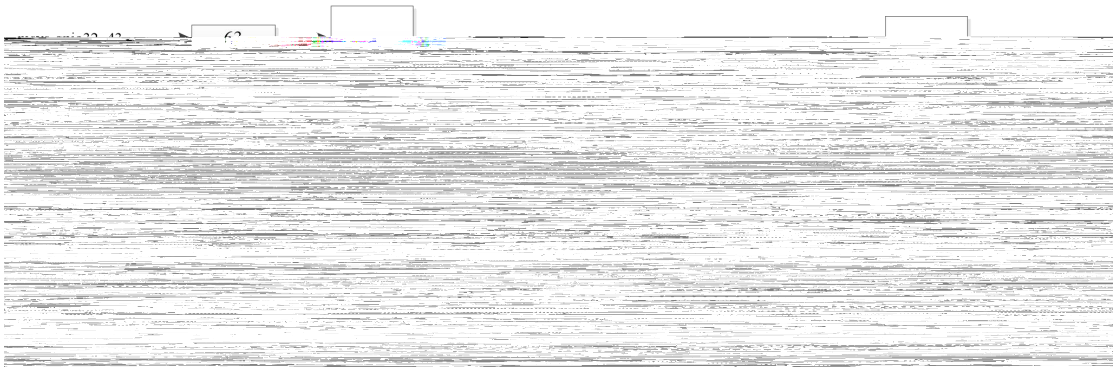
0x14001148	EXTIOI_ACK	
0x140014c0	EXTIOI_MAP	
0x14001600	EXTIOI_IEN0	0
0x14001604	EXTIOI_IEN1	1
0x14001608	EXTIOI_IEN2	2
0x1400160c	EXTIOI_IEN3	3
0x14001640	EXTIOI_POL0	0
0x14001644	EXTIOI_POL1	1
0x14001648	EXTIOI_POL2	2
0x1400164c	EXTIOI_POL3	3
0x14001700	EXTIOI_ISR0/ICLR0	/ 0
0x14001704	EXTIOI_ISR1/ICLR1	/ 1
0x14001708	EXTIOI_ISR2/ICLR2	/ 2
0x1400170c	EXTIOI_ISR3/ICLR3	/ 3
0x14001800	EXTIOI_CORE_ISR0/ICLR0	CORE / 0
0x14001804	EXTIOI_CORE_ISR1/ICLR1	CORE / 1
0x14001808	EXTIOI_CORE_ISR2/ICLR2	CORE / 2
0x1400180c	EXTIOI_CORE_ISR3/ICLR3	CORE / 3

5- 92 IO

0x15103400	PRT_INT_ISR0	0
0x15103404	PRT_INT_IEN0	0
0x1510340c	PRT_INT_CLR0	0
0x15103410	PRT_INT_POL0	0
0x15103414	PRT_INT_EDGE0	0
0x15103418	PRT_INT_DUAL0	0
0x15103420	PRT_INT_ISR1	1
0x15103424	PRT_INT_IEN1	1
0x1510342c	PRT_INT_CLR1	1
0x15103430	PRT_INT_POL1	1
0x15103434	PRT_INT_EDGE1	1
0x15103438	PRT_INT_DUAL1	1
0x15103440	PRT_INT_ISR2	2
0x15103444	PRT_INT_IEN2	2
0x1510344c	PRT_INT_CLR2	2
0x15103450	PRT_INT_POL2	2
0x15103454	PRT_INT_EDGE2	2
0x15103458	PRT_INT_DUAL2	2
0x15103460	PRT_INT_MAP0	0
0x15103464	PRT_INT_MAP1	1
0x15103468	PRT_INT_MAP2	2
0x1510346c	PRT_INT_MAP3	3
0x15103470	PRT_INT_MAP4	4
0x15103474	PRT_INT_MAP5	5

96

10



5- 5 10

5- 93 I0

0x15202400	SCA_INT_ISR0	0
0x15202404	SCA_INT_IEN0	0
0x1520240c	SCA_INT_CLR0	0
0x15202410	SCA_INT_POL0	0
0x15202414	SCA_INT_EDGE0	0
0x15202418	SCA_INT_DUAL0	0
0x15202420	SCA_INT_ISR1	1
0x15202424	SCA_INT_IEN1	1
0x1520242c	SCA_INT_CLR1	1
0x15202430	SCA_INT_POL1	1
0x15202434	SCA_INT_EDGE1	1
0x15202438	SCA_INT_DUAL1	1
0x15202440	SCA_INT_ISR2	2
0x15202444	SCA_INT_IEN2	2
0x1520244c	SCA_INT_CLR2	2
0x15202450	SCA_INT_POL2	2
0x15202454	SCA_INT_EDGE2	2
0x15202458	SCA_INT_DUAL2	2
0x15202460	SCA_INT_MAP0	0
0x15202464	SCA_INT_MAP1	1
0x15202468	SCA_INT_MAP2	2
0x1520246c	SCA_INT_MAP3	3
0x15202470	SCA_INT_MAP4	4
0x15202474	SCA_INT_MAP5	5

5.5.2

5.5.3

5- 94

	/						
	Intedge	Inten	Intenset	Intenclr	Intpol	Intentry	
0	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	MSYS_UART00
1	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	MSYS_UART01
2	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	MSYS_UART02
3	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	MSYS_UART03
4	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	MSYS_I2C0
5	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	MSYS_I2C1
6	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	MSYS_SPI1
7	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	MSYS_GMAC0_WK
8	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	MSYS_HPET0

	/						
	Intedge	Inten	Intenset	Intenclr	Intpol	Intentry	
9	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	MSYS_HPET1
10	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	MSYS_PM2IO
11	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	MSYS_PWM0~7
12	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	MSYS_PWM8~15
13	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	MSYS_SDIO0~1
14	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	MSYS_SDIO0/1-DMA
15	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	MSYS_ENCRYPT-DMA
16	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	MSYS_ENCRYPT-DEV
17	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	MSYS_OTG
18	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	MSYS_GMAC0
19	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	MSYS_SPI0
20	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	MSYS_EHCI
21	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	MSYS_OHCI
22	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	MSYS_GMAC1
23	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	MSYS_JBIG
24	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	MSYS_JPEG
25	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	MSYS_THSENS
26	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	MSYS_PRMLB
27	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	MSYS_SCMLB
28	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	MSYS_GPIO0~15
29	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	MSYS_GPIO16~31
30	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	MSYS_GPIO32~43
31	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	Reserved
32	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	PRSYS_PRMLB
33	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	PRSYS_SCMLB
34	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	Reserved
35	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	PRSYS_PWM
36	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	PRSYS_SPI
37	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	PRSYS_HPET
38	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	PRSYS_I2C
39	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	PRSYS_UART
40	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	PRSYS_RTC_TICK
41	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	PRSYS_TOY_TICK
42	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	PRSYS_INT_RTC
43	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	PRSYS_INT_TOY
44	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	PRSYS_PRTIFC

	/						
	Intedge	Inten	Intenset	Intenclr	Intpol	Intentry	
45	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	PRSYS_PM0I0
46	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	Reserved
47	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	PRSYS_GPI00~23
48	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	PRSYS_GPI024~47
49	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	PRSYS_GPI048~57
50	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	Reserved
51	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	SCSYS_SCMLB
52	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	SCSYS_PRMLB
53	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	SCSYS_UART0
54	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	SCSYS_UART1
55	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	SCSYS_SPI
56	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	SCSYS_PM1I0
57	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	SCSYS_HPET
58	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	SCSYS_SCIFC
59	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	SCSYS_GPI00~7
60	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	SCSYS_GPI08~15
61	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	SCSYS_GPI016~23
62	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	SCSYS_GPI024~31
63	RW / 0	R / 0	W / 0	W / 0	RW / 0	RW / 0	SCSYS_GPI032~36

5- 95

Intisr_0	0x14001420	RO	NA	32
Inten_0	0x14001424	RO	NA	32
Intenset_0	0x14001428	WO	NA	32
Intenclr_0	0x1400142c	WO	NA	32
Intpol_0	0x14001430	WO	0x0	32 1 0
Intedge_0	0x14001434	WO	0x0	32 1 0
Intisr_1	0x14001460	RO	NA	32
Inten_1	0x14001464	RO	NA	32
Intenset_1	0x14001468	WO	NA	32
Intenclr_1	0x1400146c	WO	NA	32
Intpol_1	0x14001470	WO	0x0	32 1 0
Intedge_1	0x14001474	WO	0x0	32 1 0
CORE_IPISR	0x14001000	RO	NA	IPI_Status

CORE_IPIEN	0x14001004	RW	0x0	IPI_Enalbe
CORE_IPISET	0x14001008	WO	NA	IPI_Set
CORE_IPI_CLR	0x1400100c	WO	NA	IPI_Clear
CORE_INTISR0	0x14001040	RO	NA	CORE 32
CORE_INTISR1	0x14001048	RO	NA	CORE 32

5- 96

	/					/			
	IEN	ICLR	POL			IEN	ICLR	POL	
0	R / 0	W / 0	RW / 0	MSYS_UART00	82	R / 0	W / 0	RW / 0	Reserved
1	R / 0	W / 0	RW / 0	MSYS_UART01	83	R / 0	W / 0	RW / 0	PRSYS_PWM0~7
2	R / 0	W / 0	RW / 0	MSYS_UART02	84	R / 0	W / 0	RW / 0	PRSYS_PWM8~15
3	R / 0	W / 0	RW / 0	MSYS_UART03	85	R / 0	W / 0	RW / 0	PRSYS_PWM16~23
4	R / 0	W / 0	RW / 0	MSYS_I2C0	86	R / 0	W / 0	RW / 0	PRSYS_SPI
5	R / 0	W / 0	RW / 0	MSYS_I2C1	87	R / 0	W / 0	RW / 0	PRSYS_HPET_CNT0
6	R / 0	W / 0	RW / 0	MSYS_SPI1	88	R / 0	W / 0	RW / 0	PRSYS_HPET_CNT1/2
7	R / 0	W / 0	RW / 0	MSYS_ENCRYPT-DMA	89	R / 0	W / 0	RW / 0	PRSYS_I2C0
8	R / 0	W / 0	RW / 0	MSYS_SDIO0	90	R / 0	W / 0	RW / 0	PRSYS_I2C1
9	R / 0	W / 0	RW / 0	MSYS_SDIO0_DMA	91	R / 0	W / 0	RW / 0	PRSYS_UART0
10	R / 0	W / 0	RW / 0	MSYS_SDIO1	92	R / 0	W / 0	RW / 0	PRSYS_UART1
11	R / 0	W / 0	RW / 0	MSYS_SDIO1_DMA	93	R / 0	W / 0	RW / 0	PRSYS_RTC_TICK
12	R / 0	W / 0	RW / 0	MSYS_HPET0_CNT0	94	R / 0	W / 0	RW / 0	PRSYS_TOY_TICK
13	R / 0	W / 0	RW / 0	MSYS_HPET0_CNT1	95	R / 0	W / 0	RW / 0	PRSYS_INT_RTC0
14	R / 0	W / 0	RW / 0	MSYS_HPET0_CNT2	96	R / 0	W / 0	RW / 0	PRSYS_INT_RTC1
15	R / 0	W / 0	RW / 0	MSYS_HPET1_CNT0	97	R / 0	W / 0	RW / 0	PRSYS_INT_RTC2
16	R / 0	W / 0	RW / 0	MSYS_HPET1_CNT1	98	R / 0	W / 0	RW / 0	PRSYS_INT_TOY0
17	R / 0	W / 0	RW / 0	MSYS_HPET1_CNT2	99	R / 0	W / 0	RW / 0	PRSYS_ INT_TOY1
18	R / 0	W / 0	RW / 0	MSYS_PM2IO	100	R / 0	W / 0	RW / 0	PRSYS_ INT_TOY2
19 20 ~ 34	R / 0	W / 0	RW / 0	MSYS_PWM0 MSYS_PWM1 ~ MSYS_PWM15	101	R / 0	W / 0	RW / 0	PRSYS_PRTIFC
35	R / 0	W / 0	RW / 0	MSYS_AES	102	R / 0	W / 0	RW / 0	PRSYS_PM0IO
36	R / 0	W / 0	RW / 0	MSYS_DES	103	R / 0	W / 0	RW / 0	Reserved
37	R / 0	W / 0	RW / 0	MSYS_SM3	104	R / 0	W / 0	RW / 0	PRSYS_GPIO0~23
38	R / 0	W / 0	RW / 0	MSYS_SM4	105	R / 0	W / 0	RW / 0	PRSYS_GPIO24~47
39	R / 0	W / 0	RW / 0	MSYS_OTG	106	R / 0	W / 0	RW / 0	PRSYS_GPIO48~57

	/				/			
	IEN	ICLR	POL			IEN	ICLR	POL	
40	R / 0	W / 0	RW / 0	MSYS_GMAC0	112	R / 0	W / 0	RW / 0	SCSYS_SCMLB
41 42 ~ 51	R / 0	W / 0	RW / 0	MSYS_GPIO00~03 MSYS_GPIO04~07 ~ MSYS_GPIO40~43	113	R / 0	W / 0	RW / 0	SCSYS_PRMLB
57	R / 0	W / 0	RW / 0	MSYS_SPI0	114	R / 0	W / 0	RW / 0	SCSYS_UART0
58	R / 0	W / 0	RW / 0	MSYS_EHCI	115	R / 0	W / 0	RW / 0	SCSYS_UART1
59	R / 0	W / 0	RW / 0	MSYS_OHCI	116	R / 0	W / 0	RW / 0	SCSYS_SPI
60	R / 0	W / 0	RW / 0	MSYS_GMAC1	117	R / 0	W / 0	RW / 0	SCSYS_PM1IO
61	R / 0	W / 0	RW / 0	MSYS_JBIG	118	R / 0	W / 0	RW / 0	SCSYS_HPET
62	R / 0	W / 0	RW / 0	MSYS_JPEG	119	R / 0	W / 0	RW / 0	SCSYS_SCIFC
63	R / 0	W / 0	RW / 0	MSYS_THSENS	120	R / 0	W / 0	RW / 0	SCSYS_GPIO0~7
64	R / 0	W / 0	RW / 0	MSYS_PRMLB	121	R / 0	W / 0	RW / 0	SCSYS_GPIO8~15
65	R / 0	W / 0	RW / 0	MSYS_SCMLB	122	R / 0	W / 0	RW / 0	SCSYS_GPIO16~23
66	R / 0	W / 0	RW / 0	MSYS_GMAC0_WK	123	R / 0	W / 0	RW / 0	SCSYS_GPIO24~31
80	R / 0	W / 0	RW / 0	PRSYS_PRMLB	124	R / 0	W / 0	RW / 0	SCSYS_GPIO32~36
81	R / 0	W / 0	RW / 0	PRSYS_SCMLB					

5- 97 IO

	/					
	Intedge	Inten	Intclr	Intpol	Intdual	
0	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	PRSYS_PRMLB
1	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	PRSYS_SCMLB
2	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	Reserved
3	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	PRSYS_PWM00~03
4	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	PRSYS_PWM04~07
5	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	PRSYS_PWM08~11
6	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	PRSYS_PWM12~15
7	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	PRSYS_PWM16~19
8	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	PRSYS_PWM20~23
10	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	PRSYS_SPI
11	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	PRSYS_HPET_CNT0
12	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	PRSYS_HPET_CNT1
13	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	PRSYS_HPET_CNT2
14	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	PRSYS_I2C0
15	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	PRSYS_I2C1
16	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	PRSYS_UART0

	/					
	Intedge	Inten	Intclr	Intpol	Intdual	
17	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	PRSYS_UART1
18	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	PRSYS_RTC_TICK
19	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	PRSYS_TOY_TICK
20	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	PRSYS_INT_RTC0
21	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	PRSYS_INT_RTC1
22	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	PRSYS_INT_RTC2
23	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	PRSYS_INT_TOY0
24	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	PRSYS_INT_TOY1
25	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	PRSYS_INT_TOY2
26	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	PRSYS_PRTIFC
27	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	PRSYS_PM0IO
28	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	Reserved
32 33 ~ 51	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	PRSYS_GPIO00~02 PRSYS_GPIO03~05 ~ PRSYS_GPIO57
52~63	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	Reserved
64	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	MSYS_UART00~03
65	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	MSYS_I2C0~1
66	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	MSYS_SPI0~1
67	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	MSYS_HPET
68	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	MSYS_PM2IO
69	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	MSYS_PWM0~15
70	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	MSYS_SDIO0~1
71	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	MSYS_ SDIO0/1_DMA
72	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	MSYS_ENCRYPT_DMA
73	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	MSYS_ ENCRYPT_DEV
74	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	MSYS_OTG
75	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	MSYS_GMAC0
76	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	MSYS_GMAC0_WK
77	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	MSYS_THSENS
78	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	MSYS_GPIO0~31
79	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	MSYS_GPIO32~43
80	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	SCSYS_SCMLB
81	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	SCSYS_PRMLB
82	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	SCSYS_UART0

	/					
	Intedge	Inten	Intclr	Intpol	Intdual	
83	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	SCSYS_UART1
84	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	SCSYS_SPI
85	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	SCSYS_PM1IO
86	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	SCSYS_HPET
87	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	SCSYS_SCIFC
88	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	SCSYS_GPIO0~7
89	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	SCSYS_GPIO8~15
90	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	SCSYS_GPIO16~23
91	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	SCSYS_GPIO24~31
92	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	SCSYS_GPIO32~36
93	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	Reserved

5- 98

int0_src	0x0	R	0	0
int0_en	0x4	R/W	0	0
int0_clr	0xc	W	-	0 1
int0_pol	0x10	R/W	0	0 0- 1-
int0_edge	0x14	R/W	0	0 0- 1-
int0_dual	0x18	R/W	0	0
Int1_src	0x20	R	0	1
Int1_en	0x24	R/W	0	1
Int1_clr	0x2c	W	-	1 1
Int1_pol	0x30	R/W	0	1 0- 1-
Int1_edge	0x34	R/W	0	1 0- 1-
Int1_dual	0x38	R/W	0	1
Int2_src	0x40	R	0	2
Int2_en	0x44	R/W	0	2
Int2_clr	0x4c	W	-	2 1
Int2_pol	0x50	R/W	0	2 0-

				1-		
Int2_edge	0x54	R/W	0	2	0-	1-
Int2_dual	0x58	R/W	0	2		
				96	4	
				192	2	
Int_map0	0x60			1		
~	~	R/W	0	00:	0 خط	
Int_map5	0x74					

	/					
	Intedge	Inten	Intclr	Intpol	Intdual	
56	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	MSYS_ENCRYPT_DMA
57	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	MSYS_ ENCRYPT_DEV
58	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	MSYS_OTG
59	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	MSYS_GMAC0
60	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	MSYS_GMAC0_WK
61	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	MSYS_THSENS
62	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	MSYS_GPIO0~31
63	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	MSYS_GPIO32~43
64	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	PRSYS_PRMLB
65	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	PRSYS_SCMLB
66	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	Reserved
67	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	PRSYS_PWM0~7
68	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	PRSYS_PWM8~15
69	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	PRSYS_PWM16~23
70	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	PRSYS_SPI
71	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	PRSYS_HPET_CNT0
72	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	PRSYS_HPET_CNT1/2
73	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	PRSYS_I2C0
74	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	PRSYS_I2C1
75	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	PRSYS_UART0
76	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	PRSYS_UART1
77	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	PRSYS_RTC_TICK
78	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	PRSYS_TOY_TICK
79	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	PRSYS_INT_RTC0
80	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	PRSYS_INT_RTC1
81	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	PRSYS_INT_RTC2
82	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	PRSYS_INT_TOY0
83	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	PRSYS_ INT_TOY1
84	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	PRSYS_ INT_TOY2
85	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	PRSYS_PRTIFC
86	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	PRSYS_PM0IO
87	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	Reserved
88	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	PRSYS_GPIO0~23
89	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	PRSYS_GPIO24~47
90	RW / 0	RW / 0	W / 0	RW / 0	RW / 0	PRSYS_GPIO48~57

5- 100

int0_src	0x0	R	0	0
int0_en	0x4	R/W	0	0
int0_clr	0xc	W	-	0 1
int0_pol	0x10	R/W	0	0 0- 1-
int0_edge	0x14	R/W	0	0 0- 1-
int0_dual	0x18	R/W	0	0
Int1_src	0x20	R	0	1
Int1_en	0x24	R/W	0	1
Int1_clr	0x2c	W	-	1 1
Int1_pol	0x30	R/W	0	1 0- 1-
Int1_edge	0x34	R/W	0	1 0- 1-
Int1_dual	0x38	R/W	0	1
Int2_src	0x40	R	0	2
Int2_en	0x44	R/W	0	2
Int2_clr	0x4c	W	-	2 1
Int2_pol	0x50	R/W	0	2 0- 1-
Int2_edge	0x54	R/W	0	2 0- 1-
Int2_dual	0x58	R/W	0	2
Int_map0 ~ Int_map5	0x60 ~ 0x74	R/W	0	96 4 192 2 1 00: 0 01: 1 10: 2 11: 3

5.5.4

5- 101

3:0	
7:4	0001 0 0010 1 0100 2 1000 3

5- 102

Entry0	0x14001400	MSYS_UART00	Entry32	0x14001440	PRSYS_PRMLB
Entry1	0x14001401	MSYS_UART01	Entry33	0x14001441	PRSYS_SCMLB
Entry2	0x14001402	MSYS_UART02	Entry34	0x14001442	Reserved
Entry3	0x14001403	MSYS_UART03	Entry35	0x14001443	PRSYS_PWM
Entry4	0x14001404	MSYS_I2C0	Entry36	0x14001444	PRSYS_SPI
Entry5	0x14001405	MSYS_I2C1	Entry37	0x14001445	PRSYS_HPET
Entry6	0x14001406	MSYS_SPI1	Entry38	0x14001446	PRSYS_I2C
Entry7	0x14001407	MSYS_GMAC0_WK	Entry39	0x14001447	PRSYS_UART
Entry8	0x14001408	MSYS_HPET0	Entry40	0x14001448	PRSYS_RTC_TICK
Entry9	0x14001409	MSYS_HPET1	Entry41	0x14001449	PRSYS_TOY_TICK
Entry10	0x1400140a	MSYS_PM2IO	Entry42	0x1400144a	PRSYS_INT_RTC
Entry11	0x1400140b	MSYS_PWM0~7	Entry43	0x1400144b	PRSYS_INT_TOY
Entry12	0x1400140c	MSYS_PWM8~15	Entry44	0x1400144c	PRSYS_PRTIFC
Entry13	0x1400140d	MSYS_SDIO0~1	Entry45	0x1400144d	PRSYS_PM0IO
Entry14	0x1400140e	MSYS_SDIO0/1-DMA	Entry46	0x1400144e	Reserved
Entry15	0x1400140f	MSYS_ENCRYPT-DMA	Entry47	0x1400144f	PRSYS_GPIO0~23
Entry16	0x14001410	MSYS_ENCRYPT-DEV	Entry48	0x14001450	PRSYS_GPIO24~47
Entry17	0x14001411	MSYS_OTG	Entry49	0x14001451	PRSYS_GPIO48~57
Entry18	0x14001412	MSYS_GMAC0	Entry50	0x14001452	Reserved
Entry19	0x14001413	MSYS_SPI0	Entry51	0x14001453	SCSYS_SCMLB
Entry20	0x14001414	MSYS_EHCI	Entry52	0x14001454	SCSYS_PRMLB

Entry21	0x14001415	MSYS_[illegible]CI	Entry53	0x14001455	SCSYS_UART0
Entry22	0x14001416	MSYS_[illegible]AC1	Entry54	0x14001456	SCSYS_UART1
Entry23	0x14001417	MSYS_JBIG	Entry55	0x14001457	SCSYS_SPI
Entry24	0x14001418	MSYS_JPEG	Entry56	0x14001458	SCSYS_PM1IO
Entry25	0x14001419	MSYS_THSENS	Entry57	0x14001459	SCSYS_HPET
Entry26	0x1400141a	MSYS_PRMLB	Entry58	0x1400145a	SCSYS_SCIFC
Entry27	0x1400141b	MSYS_SCMLB	Entry59	0x1400145b	SCSYS_GPIO0~7
Entry28	0x1400141c	MSYS_GPIO0~15	Entry60	0x1400145c	SCSYS_GPIO8~15
Entry29	0x1400141d	MSYS_GPIO16~31	Entry61	0x1400145d	SCSYS_GPIO16~23
Entry30	0x1400141e	MSYS_GPIO32~43	Entry62	0x1400145e	SCSYS_GPIO24~31
Entry31	0x1400141f	Reserved	Entry63	0x1400145f	SCSYS_GPIO32~36

5- 103

EXTIOI_MAP		
31:28		
27:24	EXT_IOI_ISR[127:96]	
	0001	0
	0010	1
	0100	2
	1000	3
23:20		
19:16	EXT_IOI_ISR[95:64]	
	0001	0
	0010	1
	0100	2
	1000	3
15:12		
11:8		

5- 104

	INT_MAP
PRSYS_INT_MAP4[31:0]	96 IO 4
PRSYS_INT_MAP3[31:0]	5 192 2 1
PRSYS_INT_MAP2[31:0]	
PRSYS_INT_MAP1[31:0]	00: 0
PRSYS_INT_MAP0[31:0]	01: 1 10: 2 11: 3

5- 105

	INT_MAP
SCSYS_INT_MAP4[31:0]	96 IO 4
SCSYS_INT_MAP3[31:0]	5 192 2 1
SCSYS_INT_MAP2[31:0]	
SCSYS_INT_MAP1[31:0]	00: 0
SCSYS_INT_MAP0[31:0]	01: 1 10: 2 11: 3

6 DDR3

2P0500 DDR3 SDRAM

6.1

6- 1

6.2 DDR3

DDR3 SDRAM

DDR3 SDRAM JESD79-3 DDR3

DDR3

1)

2)

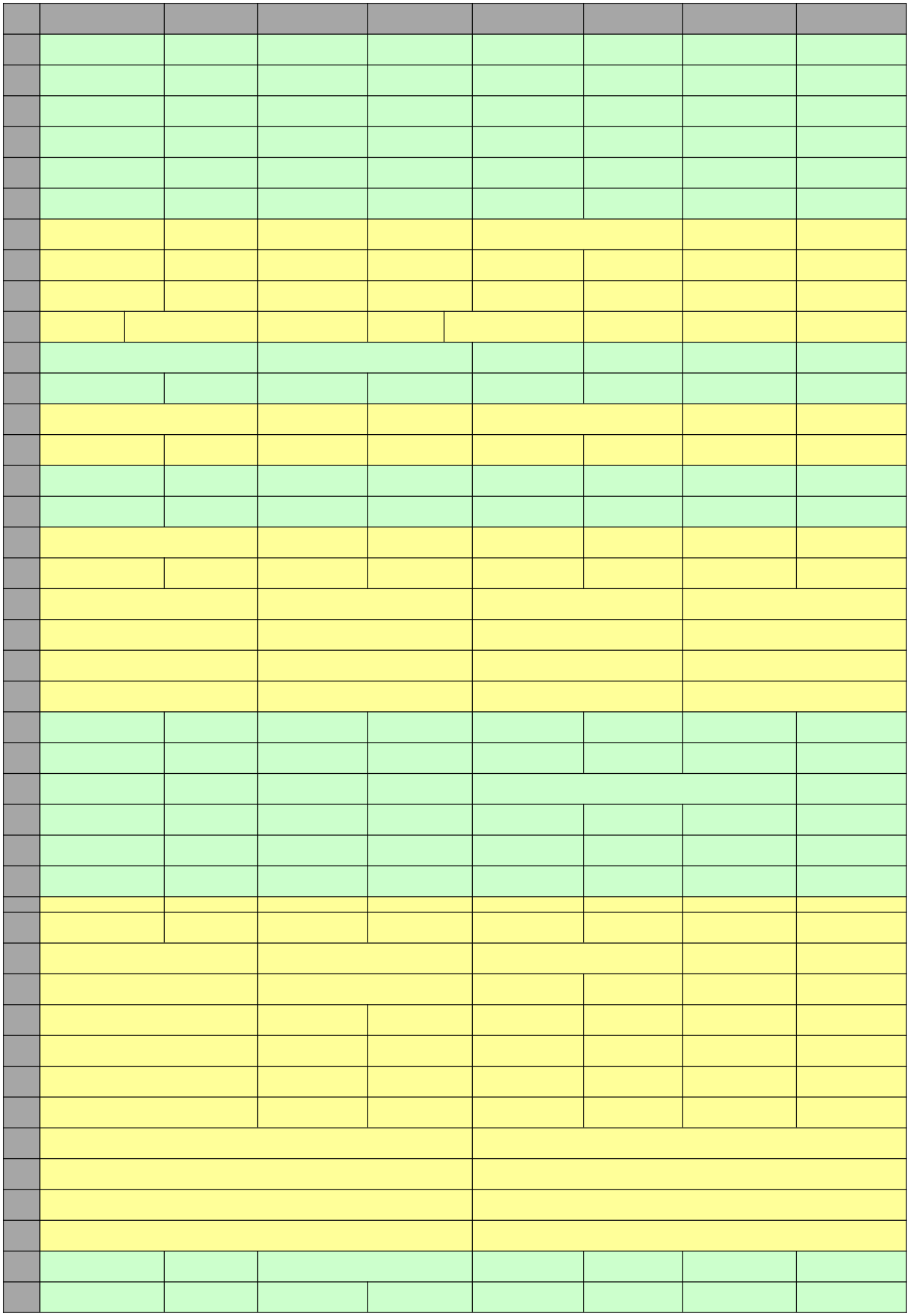
3) DDR3

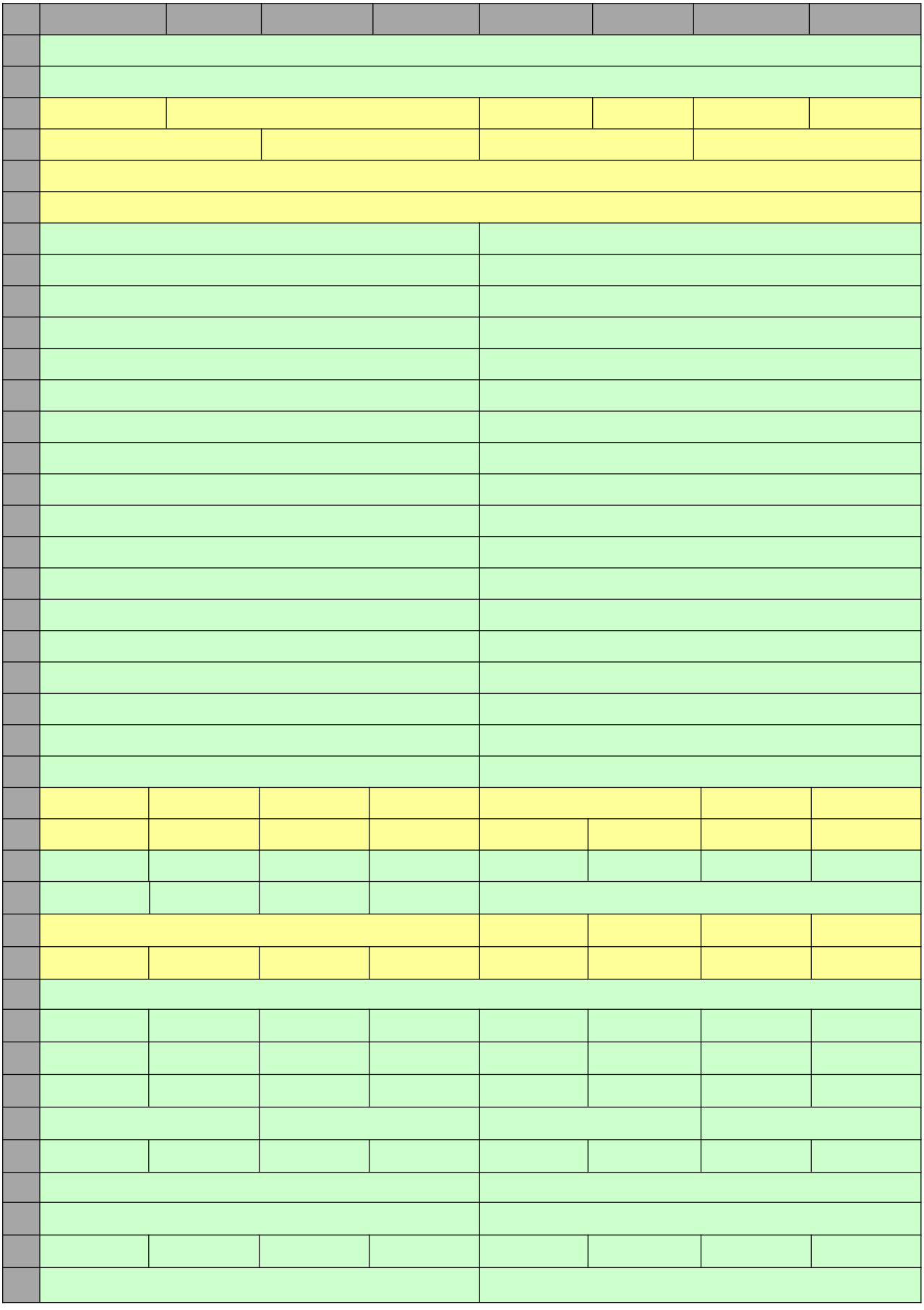
4)

2P0500 DDR3 SDRAM

0x0ff0 0000

6- 2 DDR3 SDRAM





7 GMAC

7.1

2P0500 GMAC GMAC0 GMAC1

GMAC GMAC DMA

GMAC0 GMAC 0x1414_0000 GMAC0 DMA 0x1414_1000

GMAC1 GMAC 0x1402_0000 GMAC1 DMA 0x1402_0000

7.2 :

DMA

1. (reset)GMAC
2. (DMA reg0[0])
3. DMA reg0
   a) MIX-BURST AAL(DMA reg0[26] [25])
   b) Fixed-burst undefined-burst(DMA reg0[16])
   c) Burst-length Burst-mode
   d) Descriptor Length( )
   e) Tx Rx
4. AXI Bus Mode Reg
   a) Fixed-burst burst length
5. OWN 1(DMA)
6. DMA /
7. DMA reg3 4
8. DMA reg6(DMA mode operation)
   a) / Store and Forward
   b) / (Threshold Control)
   c) (hardware flow control enable)
   d) (forwarding enable)

e) OSF

9. DMA reg6(Status reg) 1.

10. DMA reg7(interrupt enable reg) 1

11. DMA reg6[1] [13] 1 DMA

MAC

1. PHY

2. GMAC reg4(GMII Address Register) PHY

3. GMAC reg5(GMII Data Register) PHY (link) (speed) ( )

4. MAC

5. hash filtering hash filtering

6. GMAC reg1(Mac Frame filter)

a)

b) (promiscuous mode)

c) (hash or perfect filter)

d)

7. GMAC reg6(Flow control register)

a)

b)

c) /

8. (Mac reg15)

9. (link,speed,mode) GMAC reg0

10. GMAC reg0[2] [3] GMAC

1.

2. 0 OWN /

3. DMA(OWN=0) DMA DMA Tx/Rx POLL 1 DMA DMA(OWN=1)

4. buffer DMA reg18 19 20 21

8 USB

8.1

-
-
-
-

8.2

8- 1 USB

0x1403,0000 – 0x1403,7fff	EHCI	32KB
0x1403,8000 – 0x1403,ffff	OHCI	32KB

9 OTG

9.1

-
-
-
-
-
-
-
-

9.2

10 SPI-FLASH

SPI Motorola

10.1 SPI

SPI0-flash 2P0500

4 SPI SPI0 IO/memory SPI1~3 IO

SPI IO SPI Flash memory

memory 0x1c000000

SPI Flash SPI0 2P0500 4

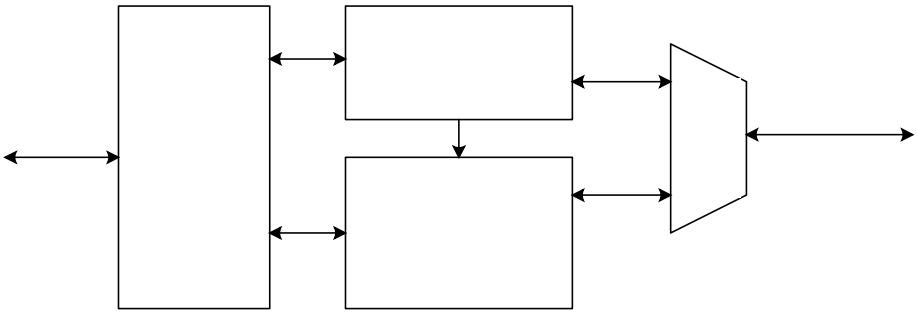
SPI

10- 1 SPI

0x1c00,0000 – 0x1c0f,ffff	SPI0 Boot	1MB
0x1000,0000 – 0x13ff,ffff	SPI0 MEM	64MB
0x1401,0000 – 0x1401,ffff	SPI0 IO/CFG	64KB
0x1420,3000 – 0x1420,3fff	SPI1 IO	4KB
0x1510,9000 – 0x1510,9fff	SPI2 IO	4KB
0x1520,3000 – 0x1520,3fff	SPI3 IO	4KB

10- 1 AXI/APB SPI SPI Flash

SPI SPI Flash ( )



10- 1 SPI

10.2

10- 2 SPI0

0	SPCR		SPI0
1	SPSR		SPI0
2	TxFIFO/RxFIFO		SPI0
3	SPER		SPI0
4	SFC_PARAM		SPI0
5	SFC_SOFTCS		SPI0
6	SFC_TIMING		SPI0

10.2.1 (SPCR)

10- 3 SPI (SPCR)

7	spie	R/W	0	
6	spe	R/W	0	
5	-	-	0	
4	mstr	-	1	master 1
3	cpol	R/W	0	
2	cpha	R/W	0	1 0
1:0	spr	R/W	0	sclk_o sper spre

10.2.2 (SPSR)

10- 4 SPI (SPSR)

7	spif	R/W	0	1 1
6	wcol	R/W	0	1 , 1
5:4	-	-	0	
3	wffull	R	0	1
2	wfempty	R	1	1
1	rffull	R	0	1
0	rfempty	R	1	1

10.2.3 (TxFIFO/RxFIFO)

10- 5 SPI (TxFIFO/RXFIFO)

7:0	TxFIFO RxFIFO	W R	-	

10.2.4 (SPER)

10- 6 SPI (SPER)

7:6	icnt	R/W	0	00: 1 01: 2 10: 3 11: 4
5:3	-	-	-	
2	mode	R/W	0	spi 0: 1:
1:0	spre	R/W	0	spr

10- 7 SPI

spre spr	00 00	00 01	00 10	00 11	01 00	01 01	01 10	01 11	10 00	10 01	10 10	10 11
	2	4	16	32	8	64	128	256	512	1024	2048	4096

10.2.5 (SFC_PARAM)

10- 8 SPI (SFC_PARAM)

7:4	clk_div	R/W	2	{spre, spr}
3	dual_io	R/W	0	I/O
2	fast_read	R/W	0	
1	burst_en	R/W	0	SPI flash
0	memory_en	R/W	1	SPI flash csn[0]

10.2.6 (SFC_SOFTCS)

10- 9 SPI (SFC_SOFTCS)

7:4	csn	R/W	0	csn
3:0	csen	R/W	0	1 csn 7:4

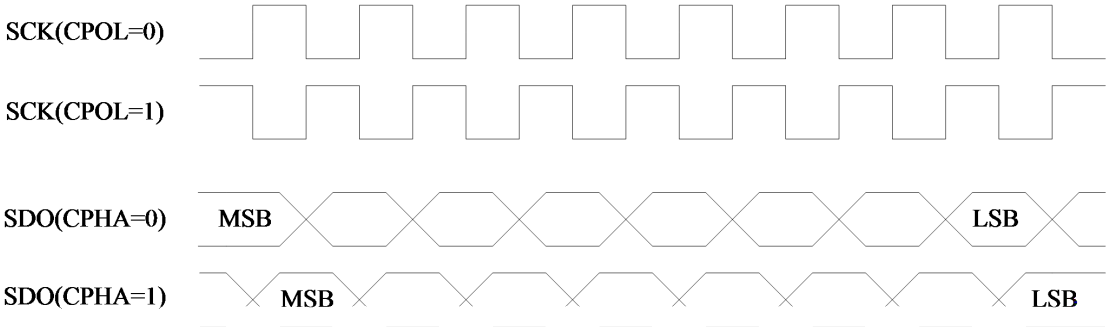
10.2.7 (SFC_TIMING)

10- 10 SPI (SFC_TIMING)

7:3	-	-	-	
2	tFAST	R/W	0	SPI flash 0: SPI 1: SPI
1:0	tCSH	R/W	3	SPI Flash T 00: 1T 01: 2T 10: 4T 11: 8T

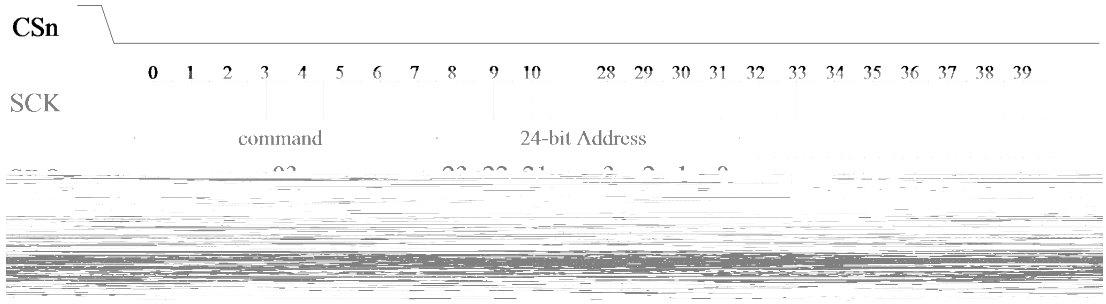
10.3

10.3.1 SPI

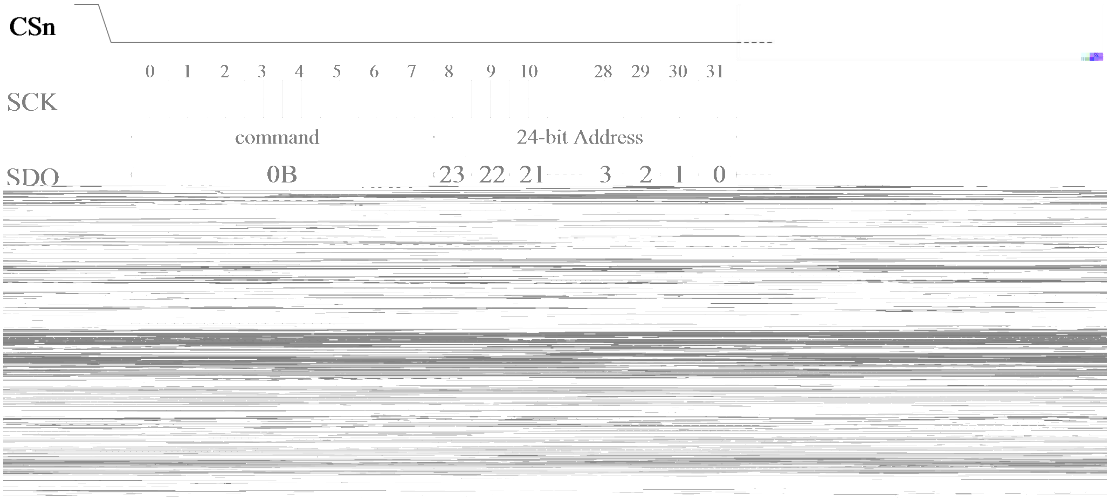


10- 2 SPI

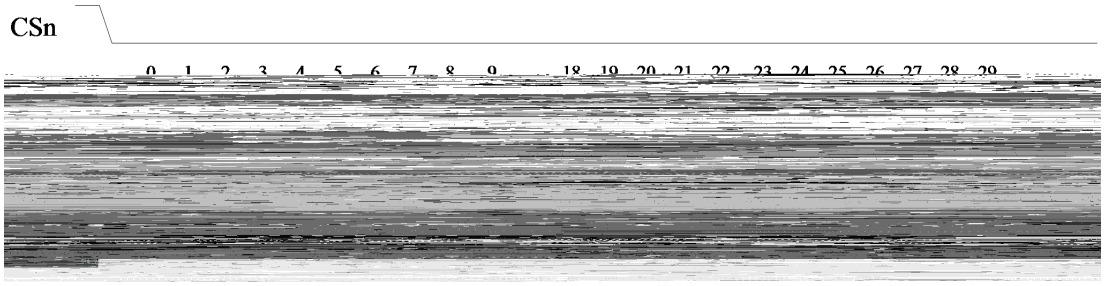
10.3.2 SPI Flash



10- 3 SPI Flash



10- 4 SPI Flash



10- 5 SPI Flash I/O

10.4

10.4.1 SPI

1.

- SPI spcr spe 0
- spsr 8'b1100_0000
- sper sper[7:6] sper[1:0]

- SPI spcr cpol cpha sper mode mode 1
  SPI 0
- spcr spie
- SPI spcr spe 1

2. /

-
-

SPI

3.

-
- spsr spsr[2] 1 spsr[0]
  1
-
- spsr spif 1

10.4.2 SPI Flash

1.

- SFC_PARAM memory_en 1 SPI 1
- (I/O tCSH)

2.

SPI Flash

Flash SPI Flash (memory_en)

10.4.3 SPI Flash SPI

1. SPI Flash

SPI Flash csn[0] SPI SPI

SPI Flash

SPI Flash ( ) Flash

11 SPI-IO

SPI Motorola

11.1 SPI

2P0500 4 SPI SPI0 IO/memory SPI1~3 IO 2P0500 3 SPI-IO

11- 1 SPI

0x1420,3000 – 0x1420,3fff	SPI1 IO	4KB
0x1510,9000 – 0x1510,9fff	SPI2 IO	4KB
0x1520,3000 – 0x1520,3fff	SPI3 IO	4KB

11.2

11- 2 SPI-IO

0x00	CR1	1
0x04	CR2	2
0x08	CR3	3
0x0c	CR4	4
0x10	IER	
0x14	SR1	1
0x18	SR2	2
0x20	CFG1	1
0x24	CFG2	2
0x28	CFG3	3
0x30	CRC1	CRC 1
0x34	CRC2	CRC 2
0x40	DR	

11.2.1 1(CR1)

11- 3 SPI 1(CR1)

31 9	-	-	0	
8	SSREV	R/W	0	SS REVerse- 0 SS 1 SS

7:3	-	-	0	
2	AUTOSUS	R/W	0	AUTOSUSpend- 0 1 CTSIZE TSIZE CTSIZE=0
1	CSTART	R/W	0	Control START of transfer- 0 1 AUTOSUS=1 CTSIZE=0 0
0	SPE	R/W	0	SPi Enable - SPI 0 DR 1 SPI CFGx CRCx

11.2.2 2(CR2)

11- 4 SPI 2(CR2)

31 16	-	-	0
15	TXDMAEN	R/W	0

11.2.4 4(CR4)

11	MODF	R	0	MODe Fault - 1 1
10	CRCE	R	0	CRC Err - CRC crc 1 1
9	UDR	R	0	UnDer Run - txfifo 1 1
8	OVR	R	0	OVer Run - rxfifo 1 1
7	SUSP	R	0	SUSPend - 1
6	-	-	0	
5	TXE	R	0	TX fifo Empty - fifo txfifo 1
4	RXE	R	0	RX fifo Empty - fifo rxfifo 1
3	-	-	0	
2	DXA	R	0	DX dr Available - dxa = rxa & txa
1	TXA	R	0	TX dr Available - txa = (txflv + (txfthlv + 1)) <= 4
0	RXA	R	0	RX dr Available - rxa = (rxflv - (rxfthlv + 1)) >= 0

11.2.7 2(SR2)

11- 9 SPI 2(SR2)

31 11	-	-	0	
10 8	TXFLV	R	0	TX Fifo LeVel - fifo txfifo 0x0~0x4
7 3	-	-	0	
2 0	RXFLV	R	0	RX Fifo LeVel - fifo rxfifo 0x0~0x4

11.2.8 1(CFG1)

11- 10 SPI 1(CFG1)

31 13	-	-	0	
12 8	DSIZE	R/W	7	Data SIZE of frame - (DSIZE + 1) bits 3 >=4bits
7	LSBFRST	R/W		LSB transfer FiRST - LSB 0 MSB 1 LSB
6 2	-	-	0	
1	CPHA	R/W	0	Clock PHAse - 0 SCK 1 SCK
0	CPOL	R/W	0	Clock POLarity - 0 SCK 1 SCK

11.2.9 2(CFG2)

11- 11 SPI 2(CFG2)

31 16	-	-	0	
15 8	BRINT	R/W	2	Baut Rate ratio INTeger - G 6 / =

3	DOE	R/W	1	Data Output Enable - 0 pin IO 1
2	DIE	R/W	1	Data Input Enable - 0 pin IO 1
1	DIOSWP	R/W	0	Data In/Output SWaP - 0 MISO MOSI MOSI MISO 1 MOSI MISO MISO MOSI
0	MSTR	R/W	0	MaSTeR - 0 SPI 1 SPI

11.2.11 CRC 1(CRC1)

11- 13 SPI CRC 1(CRC1)

31 1	CRCPOLY	R/W	0	CRC POLYnomial - crc crc crcpoly {CRCPOLY, 1'b1} CRCEN 1 crc
0	CRCEN	R/W	0	CRC ENable - crc crc

11.2.12 CRC 2(CRC2)

11- 14 SPI CRC 2(CRC2)

31 13	-	-	0	
12:8	CRCSIZE	R/W	0	CRC SIZE - crc crc (CRCSIZE+1)
7 2	-	-	0	
1	TCRCINI	R/W	0	Tx CRC INItial value - crc 0 txcrc 0 1 txcrc 1
0	RCRCINI	R/W	0	Rx CRC INItial value - crc 0 rxcrc 0 1 rxcrc 1

11.2.13 (DR)

11- 15 SPI (DR)

31 0	DR	R/W	0	Data Reg - fifo RXFIFO RXFTHLV TXFIFO apb_wstrb

11.3 DMA

11- 16 SPI-IO DMA

0x100	ISR	
0x104	IFCR	
0x110	CCR1	1
0x114	CNDTR1	1
0x11c	CMAR1	1
0x120	CCR2	2
0x124	CNDTR2	2
0x12c	CMAR2	2

11.3.1 DMA (ISR)

11- 17 SPI DMA (ISR)

31 8	-	-	0	
7	TEIF2	R	0	2
6	HTIF2	R	0	2
5	TCIF2	R	0	2
4	GIF2	R	0	2
3	TEIF1	R	0	1
2	HTIF1	R	0	1
1	TCIF1	R	0	1
0	GIF1	R	0	1

11.3.2 DMA (IFCR)

11- 18 SPI DMA (IFCR)

31 8	-	-	0	
7	CTEIF2	W	0	2
6	CHTIF2	W	0	2
5	CTCIF2	W	0	2
4	CGIF2	W	0	2
3	CTEIF1	W	0	1
2	CHTIF1	W	0	1
1	CTCIF1	W	0	1
0	CGIF1	W	0	1

11.3.3 DMA n(CCRn)

11- 19 SPI DMA n(CCRn)

31 14	-	-	0	
13 12	MSIZE_n	R/W	0	Memory SIZE of n-channel - n AXI 0 msize = 8 bits 1 msize = 16 bits 2 msize = 32 bits
11 10	-	-	0	
9 8	PSIZE_n	R/W	0	Peripheral SIZE of n-channel - n spi XFIFO 0 psize = 8 bits 1 psize = 16 bits 2 psize = 32 bits
7	MINC_n	R/W	0	Memory INCrement Mode of n-channel - n 0 n AXI NDT 1 n AXI NDT MSIZE
6	-	-	0	
5	CIRC_n	R/W	0	CIRCular Mode of n-channel - n 0 n NDT 0 1 n NDT 0 NDT 0, NDT=1 AXI
4	-	-	0	
3	TEIE_n	R/W	0	TE Interrupt Enable of n-channel - n TE 0 n TE 1 n TE
2	HTIE_n	R/W	0	HT Interrupt Enable of n-channel - n HT 0 n HT 1 n HT
1	TCIE_n	R/W	0	TC Interrupt Enable of n-channel - n TC 0 n TC 1 n TC
0	EN_n	R/W	0	Enable of n-channel - n 0 dma n 1 dma n

n=1 RX n=2 TX

11.3.4 DMA (CNDTRn)

11- 20 SPI DMA (CNDTRn)

31 16	-	-	0	
15 0	NDT_n	R/W	0	Number of Data to Transfer n-channel - n 0 CIRC_n=1 0 NDT_n

n=1 RX n=2 TX

11.3.5 DMA (CMARn)

11- 21 SPI DMA (CMARn)

31 16	-	-	0	
15 0	MA_n	R/W	0	Memory Address n-channel - n axi MINC_n NDT

n=1 RX n=2 TX

12 I2C

12.1

I2

12.3 I2C

I2C I2C-0~3

I2C-0	0X14201000	2KB
I2C-1	0X14201800	2KB
I2C-2	0X15101000	2KB
I2C-3	0X15101800	2KB

12- 1 I2C

0x00	PRERlo	
0x01	PRERhi	
0x02	CTR	
0x03	TXD/RXD	/
0x04	CR/SR	/
0x05	BLTOP	
0x07	SADDR	

I2C

I2C 2.19

GPIO

12.3.1 PRERlo

[7 0]

0x00

0xff

12- 2

7:0	PRERlo	8	RW	8

12.3.2 PRERhi

[7 0]

0x01

0xff

12- 3

7:0	PRERhi	8	RW	8

clock_s = clock_a/4*(prescale+1)

12.3.3 CTR

[7 0]

0x02

0x00

12- 4

7	EN	1	RW	1 0
6	IEN	1	RW	1
5	ms	1	RW	( ) 0 1
4	txrok	1	RW	DR 1
3	rxrok	1	RW	DR 1
2	Reserved	-	-	
1	Buslock_check_en	1	RW	buslock_top {buslock_top,16 ' b0}
0	Slv_autoreset_en	1	RW	buslock_check_en

12.3.4 / TXD/RXD

/

[7 0]

0x03

0x00

12- 5 /

7:0	TXD/RXD	8	R/W	/

12.3.5 CR

[7 0]

0x04

0x00

12- 6

7	STA	1	W	1
6	STO	1	W	1
5	RD	1	W	1
4	WR	1	W	1
3	ACK	1	W	1 NACK
2	Recover	1	W	1
1	Reserved	-	-	
0	IACK	1	W	

‘ ’

12.3.6 SR

[7 0]

0x04

0x00

12- 7

7	RxACK	1	R	0 1 NACK
6	Busy	1	R	0 1
5	AL	1	R	1
4	Slave_addressed	1	R	1

3	Slave_rw	1	R	0 1
2	BUSLOCK	1	R	1
1	TIP	1	R	1
0	IF	1	R	1

12.3.7 BLTOP

[7 0]

0x05

0xff

12- 8

7:0	Buslock_top	8	RW	{buslock_top,16 ' b0}

12.3.8 SADDR

[7 0]

0x07

0x00

12- 9

7	Reserved	-	-	
6:0	saddr	7	RW	

13

13.1

/

4

- DMA
- 1, 2, 4, 8
- sync
- sync

0x1510c000

13.2

13-1

0x0000 - 0x03ff	0 (Channel 0)	1KB
0x0400 - 0x07ff	1 (Channel 1)	1KB
0x0800 - 0x0bff	2 (Channel 2)	1KB
0x0c00 - 0x0fff	3 (Channel 3)	1KB
0x2000 - 0x20ff		256B

14

14.1

CIS LED AFE

Segment CIS AFE

4 8 16 AFE 12

12 4 DMA

- CIS CIS LED
- AFE AFE
- tag
- DMA tag
-

0x15206000

14.2

14-1 SCAN

0x0000 - 0x01ff	CIS	512B
0x0200 - 0x02ff	AFE	256B
0x0300 - 0x03ff		256B
0x0400 - 0x04ff		128B

15 PMIO

15.1

2P0500 3 IO Programmable Multifunction IO PMIO

SoC

PMIO PMIO

PMIO PMIO

PMIO PWM

1. PWM Timer Clock PWM Generator
2. FIFO
3. Access Bypass

1. PMIO PMIO
2. /

PMIO Bank PMIO Bank Bank

0x000 0x800 Bank 24 Function Unit 16

8 PMIO 0xf00

15.2

15-1 PMIO

PMIO		
0x1420_6000	Bank0	2KB
0x1420_6f00	PMIO	2KB
0x1510_8000	Bank0	2KB
0x1510_8800	Bank1	2KB
0x1510_8f00	PMIO	2KB
0x1520_4000	Bank0	2KB
0x1520_4800	Bank1	2KB
0x1520_4f00	PMIO	2KB

16 JPEG

16.1

RGB JPEG JPEG SOI
EOI DMA RGB
Zero[31:24],R[23:16],G[15:8],B[7:0] 32 Y DC
Cb Cr AC 64 Q 4096/Q
32 [12:0]
4:4:4 4:2:2 4:1:1
0x14050000

16.2

16-1 JPEG

0x00	CMD	
0x04	STS	
0x08	Q_TABLE_ADDR	
0x0c	BLOCK_OF_IMAGE	
0x10	RGB_IN_ADDR	
0x14	JPEG_OUT_ADDR	
0x18	ENCODING_BYTE	
0x1c	END_BIT_CNT	
0x20	TRAILING	

16.2.1 CMD

0x00

32'h0

16-2

31	soft_reset	RW	
31 17	-	-	
16	finish_int_en	RW	1
15 5	-	-	
4	need_load_q_tbl	RW	1 0 1

3	bit_bound	RW	1 0 1
2 1	sample_type	RW	00 4 4 4 01 4 2 2 10 4 1 1 11
0	start	RW	1

16.2.2 STS

0x04

32'h0

16-3

31 1	-	-	
0	jpeg_enc_done	RW1C	JPEG 1 1

16.2.3 Q_TABLE_ADDR

0x08

32'h0

16-4

31 4	addr	RW	16
3 0	-	-	

16.2.4 BLOCK_OF_IMAGE

0x0c

32'h0

16-5

31 0	amount	RW	R

16-6

31 4	addr	RW	RGB 16
3 0	-	-	

16.2.6 JPEG_OUT_ADDR

0x14

32'h0

16-7

31 4	addr	RW	jpeg 16
3 0	-	-	

16.2.7 ENCODING_BYTE

0x18

32'h0

16-8

31 0 a

16.3

JPEG

1 CMD = 0x10 // 4 4 4

2 STS = 0x1 //

3 Q_TABLE_ADDR = 0x0 // 0x0

4 BLOCK_OF_IMAGE = 0x1000 // RGB 4096 8*8

5 RGB_IN_ADDR = 0x200 // RGB 0x200

6 JPEG JPEG_OUT_ADDR = 0x40000 // JPEG 0x40000

7 JPEG CMD = CMD | 0x1 //

8 JPEG while(~(STS & 0x1)) //

9 JPEG ...

17 JBIG85

17.1

JBIG85 jbig85

JBIG85 4

17- 1 JBIG

0x0000	JBIG0	
0x4000	JBIG1	
0x8000	JBIG2	
0xc000	JBIG3	

JBIG85 10

17- 2 JBIG

0x0	32	jbig_top_cfg	R/W	JBIG
0x4	32	pscd_addr	R/W	JBIG
0x8	32	pscd_data_length	R/W	JBIG
0xc	32	output_addr	R/W	JBIG
0x10	1	start	R/W	JBIG
0x14	1	error_processed_reg	R/W	1
0x18	32	error_code_reg	R	
0x1c	1	apb_clear	W	JBIG
0x20	1	int_reg_clear	W	JBIG
0x24	1	int_reg	R	JBIG

(1) jbig_top_cfg

0x0

17- 3 jbig_top_cfg

31:9	Reserved	-	RO	
8	int_oen	1 ' b0	R_W	4 JBIG 1 0 4 AND 1 4 OR
7:4	int_en	4 ' b0	R_W	4 JBIG 1 0 [7] JBIG3 [6] JBIG2 [5] JBIG1 [4] JBIG0

3:0	jbig_en	4 ' b00	R/W	4 JBIG 1 0 [3] JBIG3 [2] JBIG2 [1] JBIG1 [0] JBIG0

(2) error_code_reg

0x18

JBIG s->buffer jbig85 20 jbig85 x0/y0/l0/mx/options buffer

17- 4 error_code_reg

31:24	jbig3_err_code	8 ' b0	R_W	JBIG3 [7:0]
23:16	jbig2_err_code	8 ' b0	R_W	JBIG2 [7:0]
15:8	jbig1_err_code	8 ' b0	R_W	JBIG1 [7:0]
7:0	jbig0_err_code	8 ' b0	R/W	JBIG0 s jbig85 jbig85_c_code [7:4] == 4 ' d6 [3:0] == 4 ' d1 s->buffer[1] < s->buffer[0] [3:0] == 4 ' d2 s->buffer[3]!=0 [3:0] == 4 ' d3 s->buffer[18]&0xf0 != 0 [3:0] == 4 ' d4 s->buffer[19]&80 != 0 [3:0] == 4 ' d5 s->buffer[2] == 0 [3:0] == 4 ' d6 s->x0 == 0 [3:0] == 4 ' d7 s->y0 == 0 [3:0] == 4 ' d8 s->l0 == 0 [3:0] == 4 ' d9 s->mx > 127 [7:4] == 4 ' d7 JBIG85 [3:0] == 4 ' d8 s->buffer[0] != 0 [3:0] == 4 ' d9 s->buffer[1] != 0 [3:0] == 4 ' d10 s->buffer[2] != 1 [3:0] == 4 ' d11 s->buffer[17] != 0 [3:0] == 4 ' d12 s->buffer[18] != 0 [3:0] == 4 ' d13 s->options &0x17 != 0

17.3

1

1. JBIG apb_clear jbig
2. JBIG jbig_cfg
3. JBIG pscd_addr jbig
4. JBIG pscd_length jbig
5. JBIG output_addr
6. JBIG start

2

1. int_reg 1
2. error_code_reg 0
3. int_reg_clear
4.

3

1. int_reg 1
2. error_code_reg 0
3. int_reg_clear
4.

18 UART

18.1

2P0500 8 UART APB UART MODEM

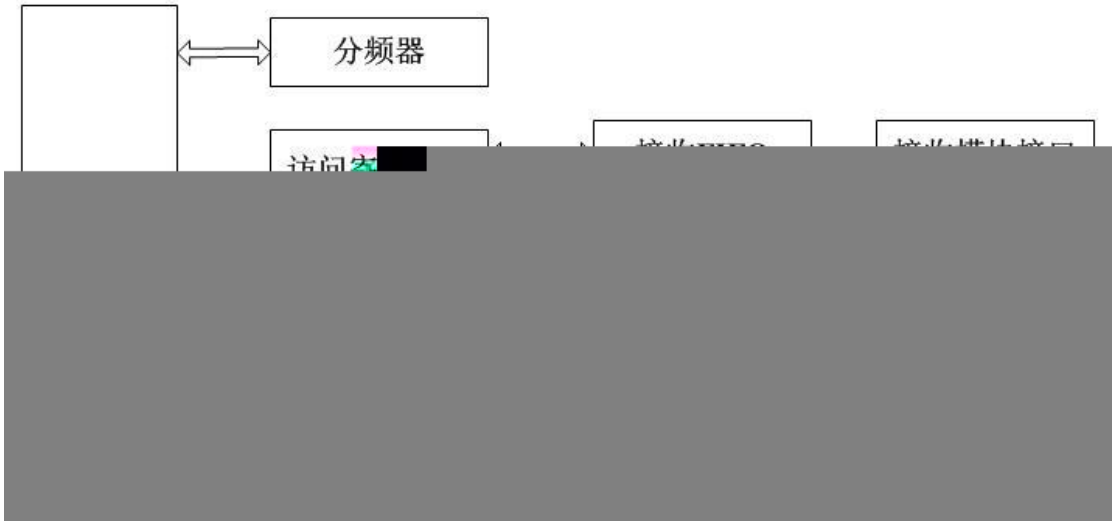
RS232

16550A

18.2

UART Transmitter and Receiver MODEM

Interrupt Arbitrator Register Access Control



18- 1 UART

1) FIFO

FIFO UART

LCR LSR

2) MODEM MODEM MCR DTR RTS MODEM

DCD,CTS,DSR RI MODEM

MSR

3) IER

1 UART UAT_INT

UART IIR

MODEM

4) UART CPU

18.3

2P0500 8 UART UART

- UART0 0x14200000
- UART1 0x14200400
- UART2 0x14200800
- UART3 0x14200c00
- UART4 0x15100000
- UART5 0x15100800
- UART6 0x15200000
- UART7 0x15200800

18- 1 UART

18.3.1 DAT

[7 0]

0x00

0x00

18- 2

7:0	Tx FIFO	8	W	

18.3.2 IER

[7 0]

0x01

0x00

18- 3

7:4	Reserved	4	RW	
3	IME	1	RW	Modem ‘0’ – ‘1’ –
2	ILE	1	RW	‘0’ – ‘1’ –
1	ITxE	1	RW	‘0’ – ‘1’ –
0	IRxE	1	RW	‘0’ – ‘1’ –

18.3.3 IIR

[7 0]

0x02

0xc1

18- 4

7:4	Reserved	4	R	
3:1	II	3	R	
0	INTp	1	R	

18- 5

Bit 3	Bit 2	Bit 1				
0	1	1	1st			LSR
0	1	0	2nd		FIFO trigger	FIFO trigger
1	1	0	2nd		FIFO 4	FIFO
0	0	1	3rd			THR IIR
0	0	0	4th	Modem	CTS, DSR, RI or DCD.	MSR

18.3.4 FIFO FCR

FIFO

[7 0]

0x02

0xc0

18- 6 FIFO

7:6	TL	2	W	FIFO trigger ‘00’ – 1 ‘01’ – 4 ‘10’ – 8 ‘11’ – 14
5:3	Reserved	3	W	
2	Txset	1	W	‘1’ FIFO
1	Rxset	1	W	‘1’ FIFO
0	Reserved	1	W	

18.3.5 LCR

[7 0]

0x03

0x03

18- 7

7	dlab	1	RW ‘1’ – ‘0’ –
6	bcb	1	RW ‘1’ – 0( ). ‘0’ –
5	spb	1	RW ‘0’ – ‘1’ – LCR[4] 1 0 LCR[4] 0 1
4	eps	1	RW

18.3.6 MODEM MCR

Modem

[7 0]

0x04

0x00

18- 8 Modem

7	Infrared	1	W	0 1
6	Rx_pol	1	W	RX 0 1
5	Infrared_pol	1	W	TX 0 1
4	Loop	1	W	‘0’ – ‘1’ – TXD 1 DTR DSR RTS CTS Out1 RI Out2 DCD
3	OUT2	1	W	DCD
2	OUT1	1	W	RI
1	RTSC	1	W	RTS
0	DTRC	1	W	DTR

18.3.7 LSR

[7 0]

0x05

0x00

18- 9

7	ERROR	1	R	‘1’ – ‘0’ –
6	TE	1	R	‘1’ – FIFO FIFO ‘0’ –
5	TFE	1	R	FIFO ‘1’ – FIFO FIFO ‘0’ –

4	BI	1	R	‘1’ – 0 ‘0’ –
3	FE	1	R	‘1’ – ‘0’ –
2	PE	1	R	‘1’ – ‘0’ –
1	OE	1	R	‘1’ – ‘0’ –
0	DR	1	R	‘0’ – FIFO ‘1’ – FIFO

LSR[4:1] LSR[7] LSR[6:5] FIFO

LSR[0] FIFO

18.3.8 MODEM MSR

Modem

[7 0]

0x06

0x00

18- 10 Modem

7	CDCD	1	R	DCD Out2
6	CRI	1	R	RI OUT1
5	CDSR	1	R	DSR DTR
4	CCTS	1	R	CTS RTS
3	DDCD	1	R	DDCD
2	TERI	1	R	RI RI
1	DDSR	1	R	DDSR
0	DCTS	1	R	DCTS

18.3.9

8

[7 0]

0x00

0x00

18- 11 8

7:0	DL_L	8	RW	8

8

[7 0]

0x01

0x00

18- 12 8

7:0	DL_H	8	RW	8

[7 0]

0x02

0x00

18- 13

7:0	DL_D	8	RW	0.45 DL_D=0x73(0x100*0.45)

UART DL_H DL_L DL_D DL UART

CLKin/16*DL 10MHz 115200 DL=5.42535 DL_H=0x0

DL_L=0x5 DL_D=0x6c(0x100*0.42535) 5%

19

19.1 DES

19.1.1

19.1.2

19.1.3

19- 1 DES

19- 2 Comand

19.2 AES

19.2.1 AES

19.2.2 AES

19.2.3 AES

19- 3 AES

0x1c	Key7	AES Key[255:224] 256-bit Key 256-bit Key AES 32
0x20	Data0	DMA (Command[2]=1 'b0): / 32 / 32 DMA (Command[2]=1 'b1):Data0-Data3
0x24	Data1	DMA (Command[2]=1 'b0): / 63 32 / 63 32 DMA (Command[2]=1 'b1):Data0-Data3
0x28	Data2	DMA (Command[2]=1 'b0): / 95 64 / 95 64 DMA (Command[2]=1 'b1):Data0-Data3
0x2c	Data3	DMA (Command[2]=1 'b0): / 32 127 96 / 32 127 96 DMA (Command[2]=1 'b1):Data0-Data3
0x30	Ctr_init_val	CTR CTR cammand[0] 0
0x34	Command	
0x38	Rev	
0x3c		

19- 4 Comand

0	0	Ctr_mode	RW	0 AES / 1 CTR AES /
1	0	decrypt	RW	0 1
2	0	dma_start	RW	1 DMA 0 DMA 1 DMA

20- 5 EMMC_PRE

			SDR 1 eMMC eMMC 0 eMMC eMMC DDR 1

20- 6 EMMC_CMD_ARG

20- 7 EMMC_CMD_ARG

20- 8 EMMC_CMD_CON

20- 9 EMMC_CMD_CON

20- 10 EMMC_CMD_STA

20- 11 EMMC_CMD_STA

20- 12 EMMC_RSP0

20- 13 EMMC_RSP0

20- 14 EMMC_RSP1

20- 15 EMMC_RESP1

20- 16 EMMC_RSP2

20- 17 EMMC_RSP2

20- 18 EMMC_RSP3

20- 19 EMMC_RSP3

20- 20 EMMC_DTIMER

20- 21 EMMC_DTIMER

20- 22 EMMC_BSIZE

20- 23 EMMC_BSIZE

20- 24 EMMC_DAT_CON

20- 25 EMMC_DAT_CON

			wide_mo

20- 26 EMMC_DAT_CNT

20- 27 EMMC_DAT_CNT

20- 28 EMMC_DAT_STA

20- 29 EMMC_DAT_STA

20- 30 EMMC_FIFO_STA

20- 31 EMMC_FIFO_STA

20- 32 EMMC_INT_MASK

20- 33 EMMC_INT_MASK

20- 34 EMMC_DAT

20- 35 EMMC_DAT

20- 36

20- 38 DLL_MASTER_VAL

/ ( )	

20- 44 SDIO_EMMC_SEL

	/ ( )	

dma_order_en DMA 64

32

DMA_SADDR

0x4
0x00000000

20- 47 DMA_SADDR

31:0	dma_saddr	32	R/W	DMA 32

DMA DMA

I2S I2S DMA

DMA 64

32

DMA_DADDR

0x8
0x00000000

20- 48 DMA_DADDR

27:0	dma_daddr	28	R/W	DMA I2S

DMA_LENGTH

0xc
0x00000000

20- 49 DMA_LENGTH

31:0	dma_length	32	R/W	

length

step length step 1

DMA

DMA_STEP_LENGTH

0x10
0x00000000

20- 50 DMA_STEP_LENGTH

31:0	dma_step_length	32	R/W	

step

step

DMA_STEP_TIMES

0x14

0x00000000

20- 51 DMA_STEP_TIMERS

31:0	dma_step_times	32	R/W	

DMA

1

DMA_CMD

0x18

0x00000000

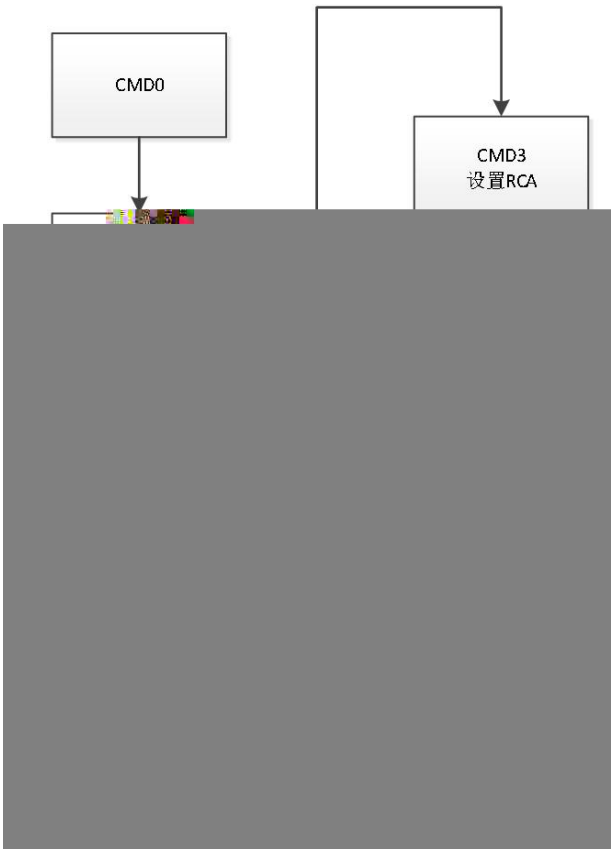
20- 52 DMA_CMD

14:13	D13:	

Write_state	[3:0]			
Write_ddr_end	4 ' h3		dma	dma
Write_dma_wait	4 ' h4	Dma	dma	
Write_dma	4 ' h5		dma	
Write_dma_end	4 ' h6		dma	
Write_step_end	4 ' h7	Dma	j	

1. emmc_con
2. emmc_pre
3. emmc_bsize
4. emmc_dtimer 100ms
5. emmc_int_en
6. emmc_ dat_con
7. bus_sel DDR SDR
8. eMMC emmc_cmd_arg emmc_cmd_con emmc_int_msk emmc_rsp0~3 EMMC
9. DMA eMMC 0x800 DMA 0x400 DMA eMMC emmc_cmd_arg emmc_cmd_con emmc_int_msk

20.5.2 eMMC



20- 1 eMMC

20.5.3 DDR

DDR eMMC eMMC DDR

DLL DDR

1.DLL pm_dll_lock_mode 1 pm_dll_start_point 0x10 0 pm_dll_adj_cnt 0xff pm_dll_increment pm_dll_bypass pm_dll_resync 1 pm_init_start 1 DLL

2.DLL DLL dll_init_done 1 DLL

3. DLL pm_dll_value 2 clk_pad_delay clk_rd_delay pm_dll_value/2 PCB clk_rd_delay

4.data_mode 1, DDR

21 SDIO

21.1

-
-
-
-
-
-

21.2

21- 1 SDIO

0x1421_0000	SDI00	32KB
0x1421_8000	SDI01	32KB

21.3

21- 2 SDI_CON

21- 3 SDI_CON

21- 10 SDI_CMD_STA

21- 11 SDI_CMD_STA

21- 12 SDI_RSP0

21- 13 SDI_RSP0

21- 14 SDI_RSP1

21- 15 SDI_RSP1

21- 16 SDI_RSP2

21- 17 SDI_RSP2

21- 18 SDI_RSP3

21- 19 SDI_RSP3

21- 20 SDI_DTIMER

21- 21 SDI_DTIMER

21- 22 SDI_BSIZE

21- 23 SDI_BSIZE

21- 24 SDI_DAT_CON

21- 25 SDI_DAT_CON

21- 26 SDI_DAT_CNT

21- 27 SDI_DAT_CNT

21- 28 SDI_DAT_STA

21- 29 SDI_DAT_STA

21- 33 SDI_INT_MASK

21- 43 param_delay

			-
			° ,

21- 44 sdio_emmc_sel

		/ ( )		

21- 45 sdio_emmc_sel

			-
			0

21.4

21.4.1 SD Memory

➢

21.4.2 SDIO

➢

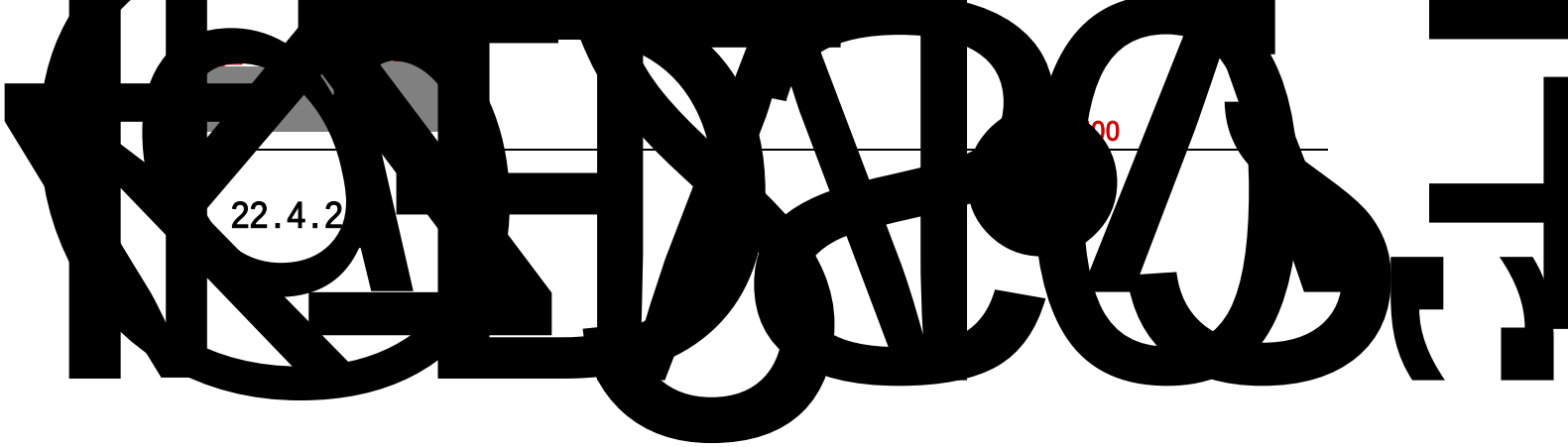
➢

➢

➢

22.4

22.4.1



22.4.2

W MMMp ǎ ضخ “

22.4.3

23 HPET

23.1

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100-107h	Timer 0 Configuration and Capability Register	R/W
108-10Fh	Timer 0 Comparator Value Register	R/W
110-11Fh	Reserved	
120-127h	Timer 1 Configuration and Capability Register	R/W
128-12Fh	Timer 1 Comparator Value Register	R/W
130-13Fh	Reserved	
140-147h	Timer 2 Configuration and Capability Register	R/W
148-14Fh	Timer 2 Comparator Value Register	R/W
150-15Fh	Reserved	

23.3.1 General Capabilities and ID Register

23- 3 General Capabilities ID

63 32	COUNTER_CLK_PERIOD	Main Counter Tick Period fps 10^-15s 0 05F5E100 100ns 10MHz	RO
31 16	VENDOR_ID		RO
15 14	Reserved		
13	COUNT_SIZE_CAP	Counter Size: 0 32 bits 1 64 bits	RO
12:8	NUM_TIM_CAP	Num of Timer GS HPET 2	RO
7:0	REV_ID	0	RO

23.3.2 General Configuaration Register

23- 4 General Configuaration

63 1	Reserved		
0	ENABLE_CNF	Overal Enable 0 0 1	R/W

23.3.3 General Interrupt Status Register

23- 5 General Interrupt Status

63 3	Reserved		
2	T2_INT_STS	Timer 2 Interrupt Active: TO_INT_STS	R/WC
1	T1_INT_STS	Timer 1 Interrupt Active: TO_INT_STS	R/WC
0	TO_INT_STS	Timer 0 Interrupt Active: 0 1. 1 0 0.	R/WC

Configuartion and Capability

Tn_TYPE_CNF

23.3.4 Main Counter Value Register

23- 6 Main Counter Value

63 32	Reserved		
31 0	Main_Counter_Val		R/W

23.3.5 Timer N Configuration and Capabilities Registe

23- 7 Timer N Configuration Capabilities

63 9	Reserved		
8	Tn_32MODE_CNF	Timer n 32-bit N 0-2 32 0	RO
7	Reserved		RO
6	Tn_VAL_SET_CNF	Timer N Value Set N 0-2 : 1 0 GS Timer 0 Timer0 Timer1 Timer2 0	R/W

5	Tn_SIZE_CAP	Timer N Size Timer N N 0-2 0 32	RO
4	Tn_PER_INT_CAP	Timer N Periodic Interrupt Capable N 0-2 : 1 0	RO
3	Tn_TYPE_CNF	Timer N type N 0-2 Tn_PER_INT_CAP 0 0. Tn_PER_INT_CAP 1, 1 0	R/W
2	Tn_INT_ENB_CNF	Timer N interrupt Enable N 0-2 :	R/W
1	Tn_INT_TYPE_CNF	Timer N Interrupt Type N 0-2 : 0 1 (General Interrupt Status Register)	
0	Reserved		

23.3.6 Timer N Comparator Value Register

23- 8 Timer N Comparator Value

63 32	Reserved		
31 0	Tn_Com_VAL	Tn_Comparator value N 0-2 ◆ ◆ ◆ 0x0123h	R/W

25

25.1

2P0500

- OTG
- Dynamic Power Management DPM NODE CORE+SCACHE DDR IMAGE SCAN SYS
- Dynamic Frequency Scaling DFS DFS LA132
-
- 3

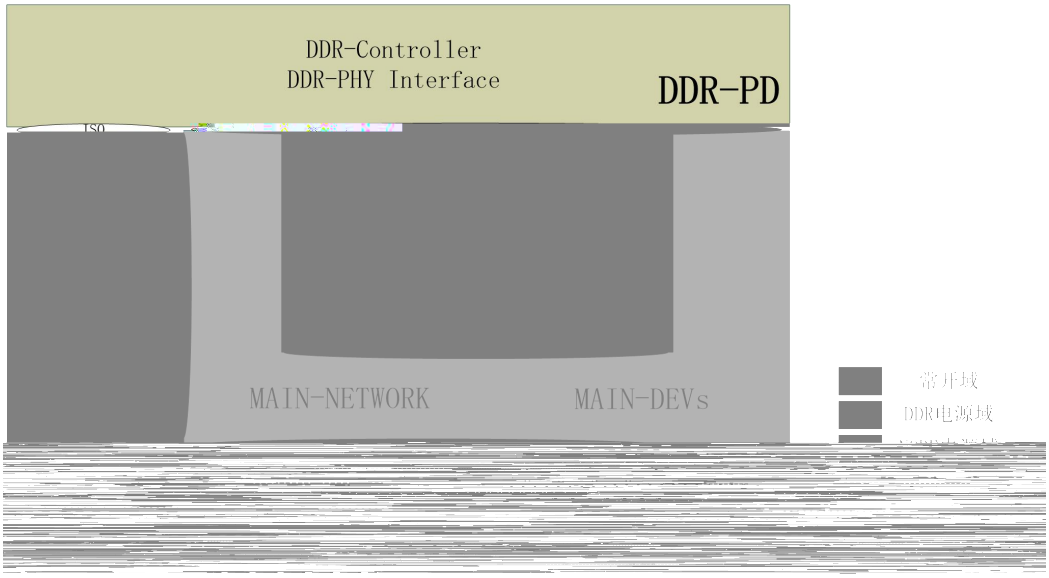
25.2

2P0500

(DFS) (DPM)

25- 1

LS2P05xx			



25- 1

25- 2

	DFS			PHY	

25.2.1 DFS

2P0500 (LA364+SCACHE) (LA132)
(LA132) (DFS) LA132

25- 2 DFS

LA132 128KB
SRAM LA132
0x15103100

2P0500 :

1 LA364 , LA132 LA364-DFS
(LA364_DFS_CTRL) LA132 LA364_DFS DFS
CLKBYP LA364 BYPASS
(100MHz) DFS_CLK_ODIV DFS_FREQSCALE
CLKBYP

2 LA132 , LA132 LA32-DFS
(LA132_DFS_CTRL) LA132 LA132_DFS DFS
CLKBYP LA132 BYPASS
(100MHz) DFS_CLK_ODIV DFS_FREQSCALE
CLKBYP

2P0500 (LA364+SCACHE) (DFS)

25- 3 DFS

2P0500

1 DFS dfs_en 2 bypass

dfs_clkbyp 3 dfs_clkodiv (1) 4 PLL

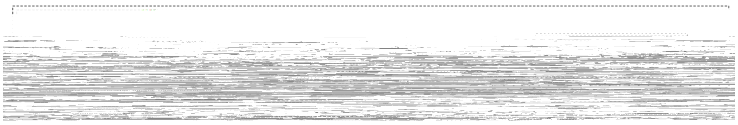
dfs_clkbyp 2P0500

2P0500

2P0500

25.2.2 DPM

2P0500 (DPM) DPM



25- 4 DPM

2P0500 (DPM)

25- 5 DPM

D0 D1

D3 (PHY PHY

)

2P0500 (D0) DPM

DPM_EN

D1 D3 DPM_TGT

DPM_STS

D1 DPM_TGT

DPM_STS WAIT_TIME

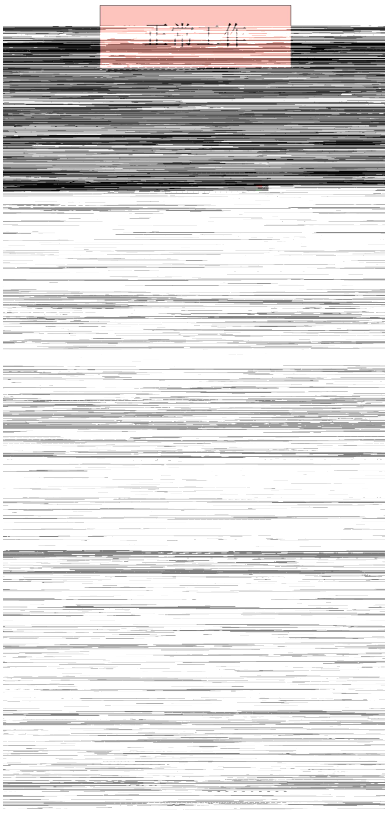
PWRUP_SEL DPM_TGT

DPM_STS

25.2.3

2P0500

OTG WIFI



25- 6

DFS DPM

OTG WIFI

DFS

DPM

25- 7

DFS

DPM

OTG WIFI

DFS DPM

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25.3

(DPM/DFS) 0x1510_4000 — 0x1510_4FFF (4KB)

R/W RO

R/WC WO

25.3.1 DPM

DPM 0x1510_4000

25.3.1.1 DPM_EN : DPM Enable Register

25- 3 DPM_EN

0x00	SOC	R/W

31:7		-
6	**IMAGE_EN – R/W** IMAGE (DPM) IMAGE DPM IMAGE	SOC
5	**RESUME_EN – R/W** RESUME (DPM) RESUME DPM RESUME	SOC
4	**SYS_EN – R/W** (DPM) DPM	SOC
3	**SCAN_EN – R/W** SCAN (DPM) SCAN DPM SCAN	SOC
2	**PRINT_EN – R/W** PRINT (DPM) PRINT DPM PRINT	SOC
1	**DDR_EN – R/W** DDR (DPM) DDR DPM DDR	SOC
0	**NODE_EN – R/W** NODE (DPM) NODE DPM NODE	SOC

25.3.1.2 PWRUP_SEL : POWERUP Select Register

25- 4 PWRUP_SEL

0x04	SOC	R/W

31:7		
6	**IMAGE_SEL – R/W** IMAGE 1 IMAGE 0 image_pwrup_time	SOC

5	**RESUME_SEL – R/W( )** RESUME 1 RESUME 0 resume_pwrup_time	SOC
4	**SYS_SEL – R/W** 1 0 sys_pwrup_time	SOC
3	**SCAN_SEL – R/W** SCAN 1 SCAN 0 scan_pwrup_time	SOC
2	**PRINT_SEL – R/W( )** PRINT 1 PRINT 0 print_pwrup_time	SOC
1	**DDR_SEL – R/W** DDR 1 DDR 0 ddr_pwrup_time	SOC
0	**NODE_SEL – R/W** NODE 1 NODE 0 node_pwrup_time	SOC

25.3.1.3 DPM_TGT : DPM Target Register

25- 5 DPM_TGT

0x08	SOC	R/W

31:14		
13:12	**IMAGE_ TGT– R/W** IMAGE 00 01 IMAGE 10 11 IMAGE	SOC
11:10	**RESUME_ TGT– R/W** RESUME 00 01 RESUME 10 11 RESUME ( )	SOC
9:8	**SYS_ TGT– R/W** 00 01 10 11	SOC
7:6	**SCAN_ TGT– R/W** SCAN 00 01 SCAN 10 11 SCAN	SOC
5:4	**PRINT_ TGT– R/W** PRINT 00 01 PRINT 10 11 PRINT ( )	SOC
3:2	**DDR_ TGT– R/W** DDR 00 01 DDR 10 11 DDR	SOC
1:0	**NODE_TGT – R/W** NODE 00 01 NODE 10 11 NODE	SOC

25.3.1.4 DPM_STS : DPM Status Register

25- 6 DPM_STS

0x0c	SOC	RO

31:14		
13:12	**IMAGE_ STS – RO** IMAGE 00 01 IMAGE 10 11 IMAGE	SOC
11:10	**RESUME_ STS – RO** RESUME 00 01 RESUME 10 11 RESUME ( )	SOC
9:8	**SYS_ STS – RO** 00 01 10 11	SOC
7:6	**SCAN_ STS – RO** SCAN 00 01 SCAN 10 11 SCAN	SOC
5:4	**PRINT_ STS – RO** PRINT 00 01 PRINT 10 11 PRINT ( )	SOC
3:2	**DDR_ STS – RO** DDR 00 01 10 11	SOC
1:0	**NODE_ STS – RO** NODE 00 01 10 11	SOC

25.3.1.5 WAIT_TIME0 : Wait Time0 Register

25- 7 WAIT_TIME0

0x10	SOC	R/W

31:24	**DDR_PWRUP_TIME – R/W** DDR 0~255	SOC
23:16	**DDR_RST_WTIME – R/W** DDR 0~255	SOC
15:8	**NODE_PWRUP_TIME – R/W** NODE 0~255	SOC
7:0	**NODE_RST_WTIME – R/W** NODE 0~255	SOC

25.3.1.6 WAIT_TIME1 : Wait Time1 Register

25- 8 WAIT_TIME1

0x14	SOC	R/W

31:24	**SCAN_PWRUP_TIME – R/W** SCAN 0~255	SOC
23:16	**SCAN_RST_WTIME – R/W** SCAN 0~255	SOC
15:8	**PRINT_PWRUP_TIME – R/W( )** PRINT 0~255	SOC
7:0	**PRT_RST_WTIME – R/W( )** PRINT 0~255	SOC

25.3.1.7 WAIT_TIME2 : Wait Time2 Register

25- 9 WAIT_TIME2

0x18	SOC	R/W

31:24	**RESUME_PWRUP_TIME – R/W( )** RESUME 0~255	SOC
23:16	**RESUME_RST_WTIME – R/W( )** RESUME 0~255	SOC
15:8	**SYS_PWRUP_TIME – R/W** 0~255	SOC
7:0	**SYS_RST_WTIME – R/W** 0~255	SOC

25.3.1.8 WAIT_TIME3 : Wait Time3 Register

25- 10 WAIT_TIME3

0x1c	SOC	R/W

31:16		
15:8	**IMAGE_PWRUP_TIME – R/W** IMAGE 0~255	SOC
7:0	**IMAGE_RST_WTIME – R/W** IMAGE 0~255	SOC

25.3.1.9 CG_CFG : Clkgate Config Register

25- 11 CG_CFG

0x20	SOC	R/W

31:23		-
22	**DDR_CG_EN – R/W** DDR (DDR DPM) 0 0 1	SOC
21	**DDR_RST_EN – R/W** DDR (DDR DPM)	SOC

0
0 1
20 **DDR_ISO_EN – R/W** SOC
DDR (DDR DPM)
0
0 1
19 **JPEG_CG_EN – R/W** SOC
JPEG (IMAGE DPM)
0
0 1
18 **JBIG_CG_EN – R/W** SOC
JBIG (IMAGE DPM)
0
0 1
17 **OTG_CG_EN – R/W** SOC
OTG (RESUME DPM)
0
0 1
16 **GMAC0_CG_EN – R/W**
GMAC0 (RESUME

	0 1	
1	**IODMA_CG_EN – R/W** IODMA (NODE DPM) 0 0 1	SOC
0	**LA364_CG_EN – R/W** LA364 (NODE DPM) 0 0 1	SOC

25.3.2 DFS

DFS 0x1510_4000

25.3.2.1 NODE_DVFS_CTRL : NODE DVFS Control Register

25- 12 NODE DVFS Control

0x30	SOC	R/W

31:20		
19:15	**DVFS_FREQSCALE – R/W** NODE PLL Freqscale PLL freqscale	SOC
14:8	**DVFS_CLK_ODIV – R/W** NODE PLL (odiv[14]) ( ) PLL ODIV[5:0] 0~63	SOC
7:3		-
2	**DVFS_CLK_OFF – R/W** NODE 0	SOC
1	**DVFS_CLKBYP – R/W** NODE BYPASS 0 1 NODE BYPASS 0 NODE PLL	SOC
0	**DVFS_EN – R/W** NODE (DFS) 0	SOC

25.3.2.2 LA132_DVFS_CTRL : LA132 DVFS Control Register

25- 13 LA132 DVFS Control

0x34	SOC	R/W

31:24		-
23:20	**SCALA132_DVFS_FREQSCALE – R/W** LA132( ) PLL Freqscale PLL freqscale	SOC
19:16	**PRTLA132_DVFS_FREQSCALE – R/W** LA132( ) PLL Freqscale PLL freqscale	SOC
15		-
14:8	**LA132_DVFS_CLK_ODIV – R/W** LA132( ) PLL (odiv[14]) ( ) PLL ODIV[5:0] 0~63	SOC

7	**SCALA1 RSTN_EN – R/W** LA132( ) 0 0- 1-	SOC
6	**CLK_EN** LA132( ) 0 0- 1-	SOC
5	**PRTLA132_RSTN_EN – R/W** LA132( ) 0 0- 1-	SOC
4	**PRTLA132_CLK_EN – R/W** LA132( ) 0 0- 1-	SOC
3		-
2	**LA132_DVFS_CLK_OFF – R/W** LA132( ) 0	SOC
1	**LA132_DVFS_CLKBYP – R/W** LA132( ) BYPASS 0 1 LA132 BYPASS 0 LA132 PLL	SOC
0	**LA132_DVFS_EN – R/W** LA132( ) (DFS) 0	SOC

25.3.3 WDT

(WDT)

25- 14 WDT

WDT		
0x1420_5000	MAIN_WDT	WDT
0x1510_3900	PRT_WDT	WDT
0x1520_2900	SCA_WDT	WDT

25.3.3.1 WD_EN : Watch Dog Enable Register

25- 15 WD_EN

25.3.3.3 WD_Timer : Watch Dog Timer Register

25- 17 WD_TIMER

0x08	SOC	R/W

31:0	watch dog 1

25.3.3.4 PLTRST_SET : Plantrst Set Register

25- 18 PLTRST_SET

0x0c	SOC	R/W

31:1	
0	Plantform Reset 0 plantform reset 1

26 RTC

26.1

RTC

RTC

RTC 32.768KHz

RTC TOY Time of Year RTC

TOY 0.1 RTC 32.768KHz

32

26.2

RTC 0x1510a000——0x1510afff 4KB

0X1510a000 32

26.2.1

26- 1 RTC

			RW	
sys_toytrim	0x20	32	RW	0
sys_toywrite0	0x24	32	W	TOY 32
sys_toywrite1	0x28	32	W	TOY 32
sys_toyread0	0x2C	32	R	TOY 32
sys_toyread1	0x30	32	R	TOY 32
sys_toymatch0	0x34	32	RW	TOY 0
sys_toymatch1	0x38	32	RW	TOY 1
sys_toymatch2	0x3C	32	RW	TOY 2
sys_rtcctrl	0x40	32	RW	TOY RTC
sys_rtctrim	0x60	32	RW	0
sys_rtcwrite0	0x64	32	W	RTC
sys_rtcread0	0x68	32	R	RTC
sys_rtcmatch0	0x6C	32	RW	RTC 0
sys_rtcmatch1	0x70	32	RW	RTC 1
sys_rtcmatch2	0x74	32	RW	RTC 2

26.2.2 SYS_TOYWRITE0

26- 2 TOY 32

31:26	TOY_MONTH	W	-	1~12
25:21	TOY_DAY	W	-	1~31
20:16	TOY_HOUR	W	-	0~23
15:10	TOY_MIN	W	-	0~59
9:4	TOY_SEC	W	-	0~59
3:0	TOY_MILLISEC	W	-	0.1 0~9

26.2.3 SYS_TOYWRITE1

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26- 5 TOY 32

31:0	TOY_YEAR	R	0	0 16383

26.2.6 SYS_TOYMATCH0/1/2

26- 6 TOY 0/1/2

31:26	YEAR	RW	0	0 16383
25:22	MONTH	RW	0	1~12
21:17	DAY	RW	0	1~31
16:12	HOUR	RW	0	0~23
11:6	MIN	RW	0	0~59
5:0	SEC	RW	0	0~59

26.2.7 SYS_RTCCTRL

26- 7 RTC 0/1/2

31:24		R	0	0
23	ERS	R	0	REN(bit13)
22:21		R	0	0
20	RTS	R	0	Sys_rtctrim
19	RM2	R	0	Sys_rtcmatch2
18	RM2	R	0	Sys_rtcmatch2
17	RM0	R	0	Sys_rtcmatch0
16	RS	R	0	Sys_rtcwrite
15		R	0	0
14		R	0	0
13	REN	R/W	0	RTC 1
12		R	0	0
11	TEN	R/W	0	TOY 1
10		R	0	0
9		R	0	0

8	EO	R/W	0	0: 32.768k 1: 32.768k
7		R	0	0
6		R	0	0
5	32S	R	0	0 32.768k 1 32.768k
4		R	0	0
3	TM2	R	0	Sys_toymatch2
2	TM1	R	0	Sys_toymatch1
1	TM0	R	0	Sys_toymatch0
0	TS	R	0	Sys_toywrite

26.2.8 SYS_RTCWRITE

26- 8 RTC

31:0	RTCWRITE	W	-	RTC

26.2.9 SYS_RTCREAD

26- 9 RTC

31:0	RTCREAD	R	0	RTC

26.2.10

26- 10 RTC 0/1/2

31:26	RTCMATCH0/1/2	RW	0	RTC 0/1/2

27 GPIO

27.1

139 GPIO GPIO

44 GPIO 58 GPIO 37

27.2

GPIO

27- 1 GPIO

0x1420_2000	MAIN_GPIO0~43	GPIO
0x1510_2000	PRT_GPIO0~57	GPIO
0x1520_1000	SCA_GPIO0~36	GPIO

GPIO GPIO GPIO_OEN GPIO

GPIO_O GPIO GPIO_I GPIO GPIO_INT_EN GPIO

GPIO_INT_POL GPIO GPIO_INT_EDGE GPIO

GPIO_INT_DUAL GPIO GPIO_INT_CLR GPIO

GPIO_INT_STS

27- 2 GPIO

27.3

GPIO

GPIO GPIO

GPIO GPIO

GPIO

GPIO

GPIO

27.4

27.4.1 GPIO

00-07h R/W

FFFFFFFFh 8

27- 6 GPIO

63:0	GPIO_OEN	R/W	GPIO[63:0] (GPIO) 0 1

800-83fh R/W

FFFFFFFFh 64

27- 7 GPIO

7:0	GPIO_OEN	R/W	GPIO[63:0] (GPIO) 0 1

27.4.2 GPIO

10-17h R/W

00000000h 8

27- 8 GPIO

63:0	GPIO_O	R/W	GPIO[63:0] (GPIO)

900-93fh R/W

00000000h 64

27- 9 GPIO

7:0	GPIO_O	R/W	GPIO[63:0](GPIO)

27.4.3 GPIO

20-27h RO

N/A 8

27- 10 GPIO

63:0	GPIO_I	RO	GPIO[63:0] (GPIO)

a00-a3fh RO

00000000h 64

27- 11 GPIO

7:0	GPIO_I	RO	GPIO[63:0] (GPIO)

27.4.4 GPIO

30-37h R/W

00000000h 8

27- 12 GPIO

63:0	GPIO_INT_EN	R/W	GPIO[63:0] 0 1

b00-b3fh R/W

00000000h 64

27- 13 GPIO

7:0	GPIO_INT_EN	R/W	GPIO[63:0](GPIO) 0 1

27.4.5 GPIO

40-47h R/W

00000000h 8

27- 14 GPIO

63:0	GPIO_INT_POL	R/W	GPIO[63:0] GPIO

c00-c3fh R/W

00000000h 64

27- 15 GPIO

7:0	GPIO_INT_POL	R/W	GPIO[63:0](GPIO) GPIO

27.4.6 GPIO

50-57h R/W

00000000h 8

27- 16 GPIO

63:0	GPIO_INT_EDGE	R/W	GPIO[63:0] POL EDGE 0 0 1 0 0 1 1 1

d00-d3fh R/W

00000000h 64

27- 17 GPIO

7:0	GPIO_INT_EDGE	R/W	GPIO[63:0](GPIO) POL EDGE 0 0 1 0 0 1 1 1

27.4.7 GPIO

60-67h R/W

00000000h 8

27- 18 GPIO

63:0	GPIO_INT_CLR	R/W	GPIO[63:0] 1 GPIO 0

e00-e3fh R/W

00000000h 64

27- 19 GPIO

7:0	GPIO_INT_CLR	R/W	GPIO[63:0](GPIO) 1 GPIO 0

27.4.8 GPIO

70-77h R/W

00000000h 8

27- 20 GPIO

63:0	GPIO_INT_STS	R/W	GPIO[63:0] 1 0

f00-f3fh R/W

00000000h 64

27- 21 GPIO

7:0	GPIO_INT_STS	R/W	GPIO[63:0](GPIO) 1 0

27.4.9 GPIO

80-87h R/W

00000000h 8

27- 22 GPIO

63:0	GPIO_INT_DUAL	R/W	GPIO[63:0] 1 0

f80-fbfh R/W

00000000h 64

27- 23 GPIO

7:0	GPIO_INT_DUAL	R/W	GPIO[63:0] (GPIO) 1 0

V1.0	
V1.01	1 3.1 3.6
V1.02	2.14 2.19 6.2 DDR 17.2 JBIG

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